Low-complexity OTFS Transmitter for ASIC Implementation using GPDK 45 nm and 90 nm Technology

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Abstract

In this work, Low-complexity OTFS Transmitter for ASIC Implementation using GPDK 45 nm and 90nm Technology. develop The orthogonal Time Frequency Space (OTFS) modulation provides high reliability in high-mobility communication such as 5G/6G vehicular and mmWave systems. This paper presents an ASIC implementation of an 8×8 OTFS transmitter using Cadence Genus tool targeting 45 nm and 90 nm CMOS technology nodes. A parallel and pipelined ISFFT-based architecture is designed using optimized FFT/IFFT blocks, trivial and non-trivial rotator reduction, and memory-based coefficient storage. Detailed synthesis results for area, power, and maximum frequency are compared between both technology nodes. The proposed ASIC design is suitable for low-power high-throughput wireless baseband engines.

Keywords: OTFS Modulation, High Mobility Communication, ASIC Implementation, FFT/IFFT, Booth Multiplier, High Throughput,

1. INTRODUCTION

In the current wireless communication standards, orthogonal frequency division multiplexing (OFDM) is used as a promising candidate technology in the quasi static frequency selective fading scenario. This happens because it i) combats the effect of inter-symbol interference (ISI) that arises due to the frequency-selective nature of the channel and ii) can be implemented with an efficient hardware architecture [1]. However, for the high-speed wireless communication scenarios, Doppler shifts come into the picture which gives rise to the inter-carrier interference (ICI) that in turn significantly degrades the performance of OFDM systems with the use of traditional transceivers [2]. Serial/parallel interference cancellation and operator perturbation techniques are e repetitive techniques for manipulating

a system of linear equations in the traditional OFDM that have been proposed to overcome this problem of ICI in [3, 4]. Furthermore,authors in [5], proposed linear and non-linear equalization techniques to eliminate the ICI. Transmit diversity and frequency domain equalization schemes were also proposed in [5, 6], for time-varying channels to improve the system performance. However, these aforementioned techniques can not completely nullify the ICI in the time-varying systems [7, 8].

It can be observed from the existing literature [14, 15], that the basic architecture of OFDM transmitter is very simple as it consists of only one transform i.e, IFFT. On the other hand, the architecture of OTFS transmitter is complex as it consists of two operations known as inverse symplectic fast Fourier transform (ISFFT) and Heisenberg transform. We further observe from [16] that i) ISFFT consists of many IFFT and FFT operations and ii) Heisenberg transform consists of only IFFT operations. In light of the above observations, we believe that the knowledge of the existing architectures of OFDM transmitter will help to build a robust architecture for OTFS transmitter. We, therefore, now discuss the existing literature related to the hardware architectures for OFDM transmitters.

2. REVIEW OF RECENT RESEARCHES

Recently, Hadani et al. [9] have proposed a novel modulation scheme known as OTFS (orthogonal time frequency space modulation) which converts the fast fading channel into almost quasi static channel by multiplexing the transmit symbols in the delay Doppler domain. Consequently, OTFS provides better bit error rate (BER) than the existing OFDM modulation scheme in high mobility scenarios [10, 11] by using the novel signal processing algorithms developed in [10, 12, 13].

To the best of our knowledge, OTFS modulation is a recently introduced two-dimensional (2D) modulation method that leverages the delay-Doppler domain for encoding information symbols, as detailed in [9]. It is noteworthy that OTFS incorporates both pre-processing and post-processing steps into conventional multi-carrier modulation schemes, resulting in enhanced bit error performance compared to traditional multi-carrier techniques. Furthermore, channel variations have been observed to be more gradual in the delay-Doppler domain as compared to the time-varying multi-path channel. This simplifies the equalizer design and allows for less frequent channel estimation in OTFS, consequently reducing the overhead overhead associated with channel estimation in rapidly changing channels [10].

To the best of the authors' knowledge, limited attention has been focused on VLSI architecture of the OTFS transceiver or its hardware implementation in FPGA, as observed in the current body of literature. The primary obstacles within this field pertain to the substantial scale of matrix inversion required for computing the final mathematical equations in OTFS. The proposed architecture has been developed to tackle these challenges. This work offers the advantage of efficiently utilizing FPGA board resources through the proposed architecture. This paper introduces an architectural solution designed for OTFS transceiver for the fading channel.

3. PROBLEM DEFINITION

- The main motive of our proposed work is to implement ASIC Implementation using GPDK 45 nm and 90nm Technology
- To improve the power and area
- The use shared FFT cores, smaller radix, or approximate methods.
- Tool/PDK access limitations.
- ISFFT/FFT cores dominate area/power..

The target lower frequency or more pipelining report realistic goals

4. PROPOSED METHOD

- Uses a pipelined Radix-22 FFT/IFFT architecture (R2MDC) instead of heavy parallel blocks.
- Replaces standard multipliers with:
  Modified Booth multipliers
  ROM-based approach (saves hardware space).
- Reduces rotators from 48 → 32, lowering complexity.
- The above mentioned OTFS Transmitter module is going to implement in
- Cadence 90nm and 45nm Technology nodes.
- The results both 90nm and 45nm Technologies are going to analyze the
- parameters of Power, Performance and Area Result: Faster, smaller, and more power-efficient design.

The proposed design makes OTFS practical by reducing hardware, saving power, and increasing throughput.

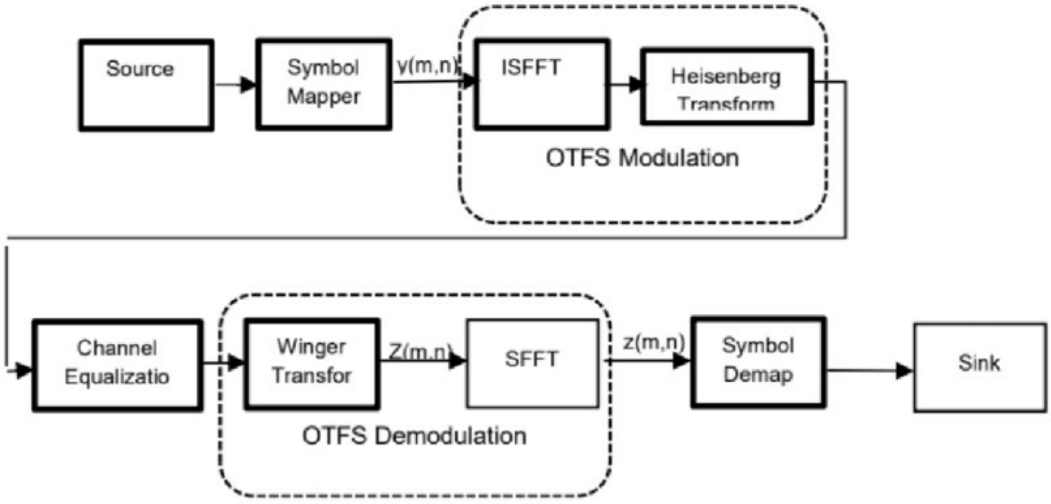


Fig.1: OTFS Modulation and Signal Transformation Using ISFFT and Heisenberg Transform

4.1 OTFS Receiver Processing

The first step in receiver processing is the **Wigner transform**, which converts the received time-domain signal into its **time–frequency representation**. The Wigner transform acts as a generalized OFDM demodulator and is the dual operation of the Heisenberg transform used at the transmitter. This step separates the signal into time–frequency samples corresponding to different subcarriers and time slots.

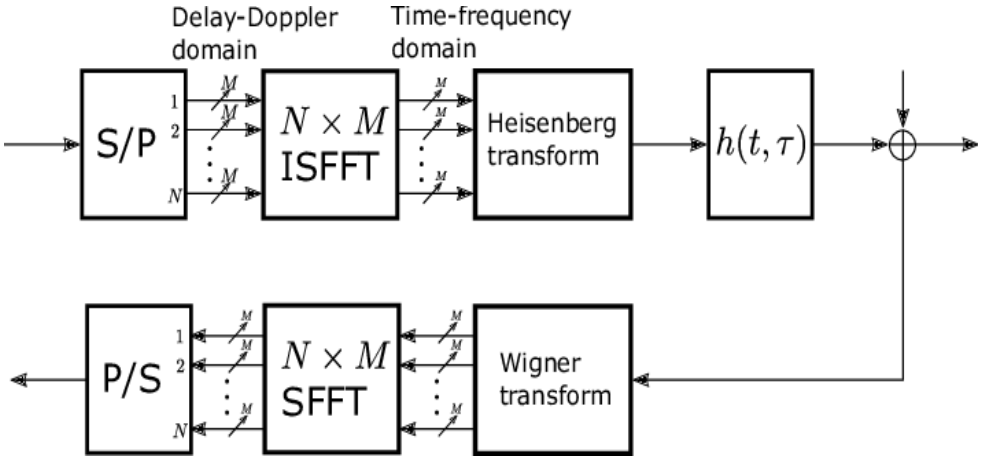
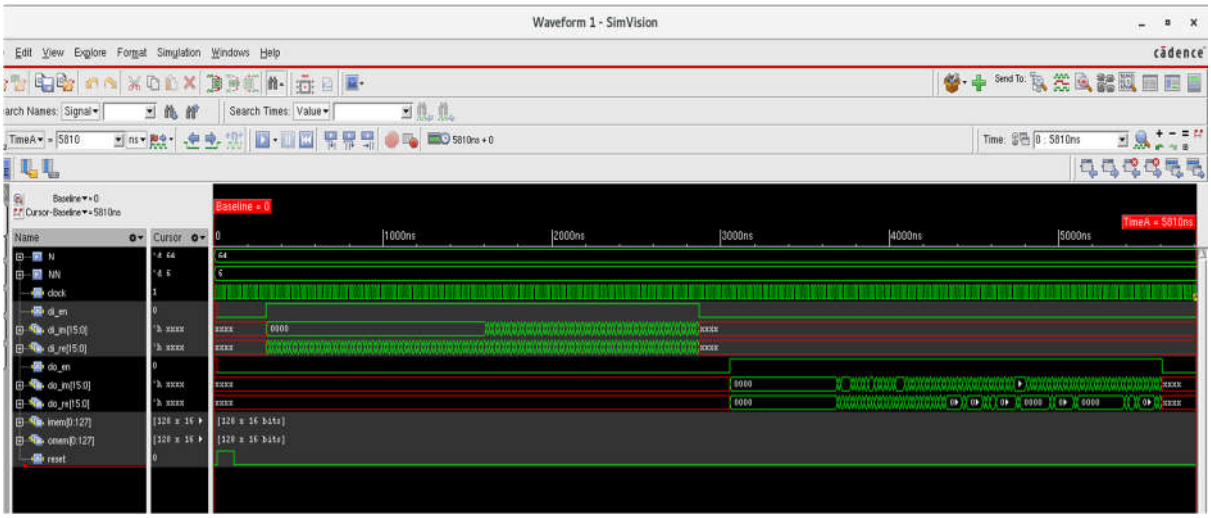


Fig 2: OTFS Receiver Processing Using Wigner Transform and SFFT

This operation converts the delay–Doppler symbols X_{dd}into time–frequency symbols X_{tf}. The time–frequency symbols are then converted into a time-domain signal using the **Heisenberg transform**, which acts as a generalized OFDM modulator. When rectangular pulse shaping is employed, the Heisenberg transform reduces to conventional OFDM modulation. This process enables OTFS to maintain compatibility with existing OFDM frameworks while achieving enhanced performance.

5. EXPERIMENTAL RESULTS

5.1 Simulated output



Graph.1 Simulation result for OTFS Transmitter

The simulated waveform represents the functional verification of the proposed OTFS transmitter architecture. The simulation was performed at the RTL level in Cadence SimVision using clock-driven event simulation.

5.2 Channel Effect in Delay–Doppler Domain

The received signal in the delay–Doppler domain is expressed as:

$$Y_{dd}[k,l] = H_{dd}[k,l] \star X_{dd}[k,l] + W_{dd}[k,l] \quad (1)$$

where:

- $H_{dd}$is the sparse delay–Doppler channel response
- $\star$denotes twisted convolution

5.3 Receivers-Side SFFT Calculation

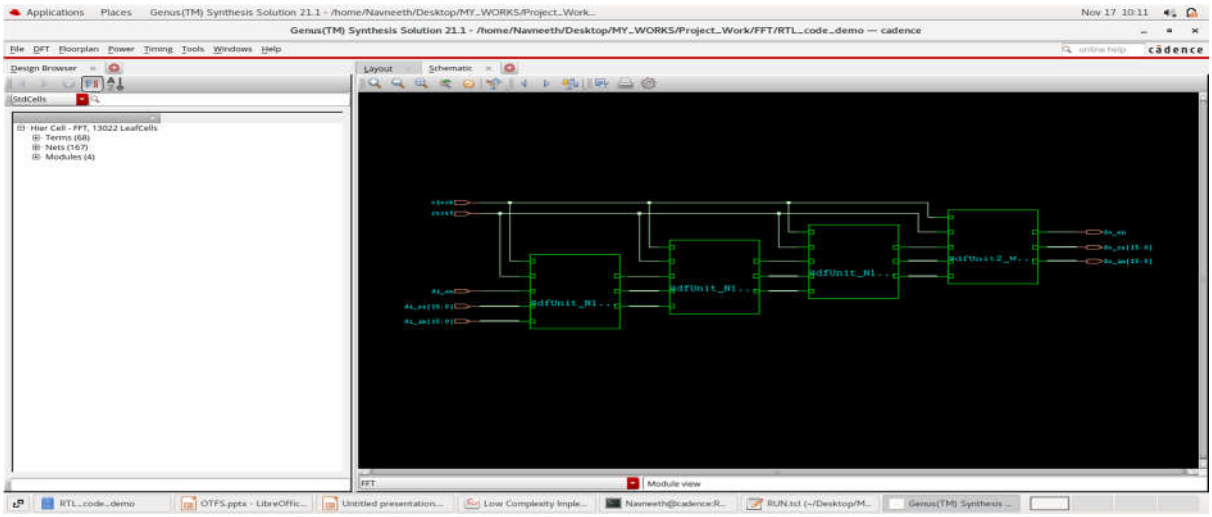
At the receiver, the Symplectic Finite Fourier Transform (SFFT) converts the time–frequency samples back into the delay–Doppler domain:

$$Y_{dd}[k,l] = \frac{1}{\sqrt{MN}} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} Y_{tf}[m,n]\, e^{-j2\pi\left(\frac{nk}{N} - \frac{ml}{M}\right)} \quad (2)$$

This operation involves:

- FFT along the Doppler dimension, and
- IFFT along the delay dimension

5.4 Synthesized Gate-Level Netlist for 90 nm Technology



Graph.2: The 90 nm technology implementation results

The 90 nm technology implementation results in lower power consumption due to the larger device dimensions and reduced leakage current. The area utilization, however, remains relatively higher because of the comparatively large transistor sizes. Overall, the 90 nm architectural mapping makes this design suitable where **low power consumption is prioritized** over silicon area, such as portable communication devices or low-energy sensor networks.

5.5 Comparison Parameter Table.1

CMOS Technology	Power (nW)	Area (um2)
90nm Technology	8.28186e-03	77394.539
45nm Technology	11.5673e-03	49700.628

Combining the waveform, synthesized netlists, and comparative analysis, it is confirmed that the designed OTFS transmitter not only functions correctly at the algorithmic level but is also

suitable for ASIC realization with optimized area and power efficiency. The transmitter can thus serve as a building block for high-mobility wireless communication systems including 5G, 6G, Intelligent Transportation Systems, and Satellite-assisted IoT.

6. CONCLUSION AND FUTURE WORK

In this paper, an optimized OTFS transmitter architecture was designed and evaluated using 90 nm and 45 nm CMOS technology nodes in Cadence EDA tools without deploying any external hardware. The synthesis results validate that the proposed architecture achieves lower power consumption in 90 nm technology and a substantial reduction in silicon area in the 45 nm implementation, demonstrating the suitability of the architecture for low-power and compact VLSI designs. Overall, the project confirms that OTFS modulation can be implemented efficiently through RTL design and ASIC synthesis flow, making it a promising physical-layer solution for high-mobility wireless communication systems in future 5G and 6G standards.The current work can be extended further to make the design more comprehensive and deployment-ready. A complete OTFS transceiver (including OTFS receiver, channel estimation, equalization, and detection blocks) can be built using the same. Support for higher-order modulation formats and migration to advanced nodes such as 28 nm, 14 nm, and 7 nm can also be explored to make the design suitable for integration into commercial SoCs for next-generation wireless communication.

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