BIST BASED PARALLEL ARCHITECTURE FOR LINEAR FEED BACK SHIFT REGISTER

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Abstract: The increasing complexity of nanoscale devices has created significant challenges in achieving efficient and reliable testing of integrated circuits. Built-In Self-Test (BIST) techniques have emerged as a promising solution to reduce external testing costs and enhance fault coverage, particularly when combined with Linear Feedback Shift Registers (LFSRs) for pseudo-random test vector generation. This paper presents a BIST-based parallel architecture for LFSRs, designed to optimize scan chain performance and improve test quality in nanoscale systems. Unlike conventional serial LFSRs, the proposed parallel structure accelerates test vector generation while reducing power consumption and test time. Additionally, LFSR test vector modification techniques are employed to minimize correlation and enhance randomness, thereby improving fault detection efficiency. The integration of scan chain optimization with modified LFSR-based BIST ensures higher reliability and scalability, making the approach suitable for advanced Very Large Scale Integration (VLSI) testing, cryptographic applications, and safety-critical nanoscale devices. Overall, the proposed methodology demonstrates a balanced trade-off between performance, area overhead and test accuracy, addressing the limitations of traditional testing strategies in emerging nanotechnology-driven circuits.

Keywords: Built-In Self-Test (BIST), Linear Feedback Shift Registers (LFSRs), Reducing Power Consumption, Very Large Scale Integration (VLSI).

I. INTRODUCTION

Built-In Self-Test (BIST) has emerged as a vital design-for-testability technique in modern digital systems, enabling circuits to test themselves without relying heavily on external testing equipment. With the increasing complexity of Very Large Scale Integration (VLSI) circuits, traditional testing methods become inefficient, time-consuming and costly. BIST provides a solution by embedding test pattern generation and output response analysis directly within the system, thus improving fault detection and reducing overall testing cost. Among various test pattern generators, the Linear Feedback Shift Register (LFSR) is one of the most widely used due to its simplicity, hardware efficiency, and ability to generate pseudo-random sequences. An LFSR is a shift register that cycle through sequences of bits generated by linear feedback logic. These sequences are used in applications such as error detection, encryption and importantly test pattern generation for BIST. The conventional LFSR architecture, while effective, often faces challenges related to power consumption, delay and scalability in parallel data processing. As VLSI systems require high-performance

and low-power testing mechanisms, modifications to the basic LFSR architecture are necessary. To address these issues, parallel architectures of LFSR have been explored, which allow multiple test patterns to be generated in a single clock cycle, thus enhancing testing speed and efficiency.

Parallel LFSR architectures are particularly useful in BIST applications where high throughput is required. By generating multiple outputs simultaneously, parallel LFSRs reduce the test application time, making them highly suitable for large-scale integrated circuits. However, the increase in parallelism must be balanced with efficient hardware design to minimize area overhead and power consumption. The incorporation of optimized feedback logic and parallel shift operations ensures that the architecture remains both compact and energy-efficient while maintaining the statistical properties of randomness required for effective fault coverage.

In BIST-based systems, the parallel LFSR serves as a core component for pseudo-random test pattern generation. It ensures a wide range of patterns, improving the chances of detecting structural and functional faults in digital circuits. Furthermore, its integration with response analyzers enables complete self-testing without external intervention. This self-sufficiency not only enhances the reliability of the system but also reduces dependency on costly Automatic Test Equipment (ATE), making it an attractive solution for modern SoCs (System on Chips) and VLSI designs.

Thus, a BIST-based parallel architecture for LFSR combines the strengths of built-in self-testing with efficient parallelism to meet the growing demands of modern integrated systems. By providing faster test application, reduced hardware cost, and lower power consumption, such architectures pave the way for scalable and robust VLSI testing solutions. The exploration of this approach is critical in designing next-generation low-power, high-performance, and self-reliable digital systems.

II. LITERATURE SURVEY

X. Zhang et al. Linear feedback shift registers (LFSRs) are used to implement BCH encoders and cyclic redundancy check (CRC), which are broadly used in digital communication systems. Previous parallel LFSR designs adopt a state-space transformation that shortens the feedback data path and reduces the gate count. Transformations have been designed to minimize the total gate count of the three involved matrix multiplications. However, the transformation matrix multiplication is only active for one clock cycle at the end. In this brief, we propose an alternative transformation matrix construction that effectively shifts the complexity from the other two matrices, which are active in every clock cycle, to the transformation matrix without increasing the critical path or the total gate count. For an example CRC-32, the proposed design achieves 33% power and 8% gate count reductions without compromising the achievable clock frequency [1].

Lingala Akhil Reddy, Gomasa Ramesh et al. Built-in Self-Test (BIST) is becoming increasingly essential in today's IC designs for memory, which is the most critical component of the System on Chip. BIST is a method for circuit design that enables it to self-test. By enabling the use of low-cost test equipment at all phases of manufacturing, the method may save time and money when compared to an externally applied test. Because of the randomization characteristics of Linear Feedback Shift Registers, this needs relatively minimal hardware (LFSRs). Linear Feedback Shift Registers have been used to create test patterns for a long time (LFSR). The feedback taps on LFSRs, which are a sequence of flip-flops linked in series, are defined by the generating polynomial. The seed value is fed into the outputs of the flip-flops. The only input needed to create a random sequence is an external clock, and each clock pulse may result in a different pattern at the flip-flops' output. The random sequence at the output of the flip-flops may be utilized as a test pattern. The number of flip-flop outputs needed by the circuit under test must match the number of inputs required by the LFSR. This test pattern is used to verify that the required fault coverage is obtained on the circuit under test. A novel low-power pattern generating method is implemented using a modified Linear Feedback Shift Register standard benchmark circuit. Using an industry standard Xilinx tool called Power analyzer or Cadence, the circuit's instantaneous and peak power consumption is examined, and it is demonstrated that the new low power method uses considerably less power than the traditional pattern for the same fault coverage. The aim of the research is to test the multipliers using a Low Power Linear Feedback Shift Resister (LFSR), which is better suited to VLSI circuit testing built-in self-test (BIST) structures. Random values are needed for testing every circuit that is developed. To do so, we create random generators that produce random values. BIST is a design for testability (DFT) method for testing that makes use of built-in hardware characteristics. Because testing is integrated into the hardware, it is quicker and more efficient. The suggested test pattern generator minimizes switching activity between test patterns, resulting in a low-cost, high-speed solution [2].

A. Mamun and R. Katti et al. Low power dissipation is very critical in today's electronic designs. Components which are widely used in design, such as sequence generators like linear feedback shift registers (LFSR), should consume as little power as possible. Two recent works on parallel architecture of LFSR, one by M. Lowy and another by M. E. Hamid and C. I. H. Chen, have reduced dynamic power consumption significantly compared to the conventional architecture and showed the way to generate multiple outputs. In this paper we propose design improvements on these parallel architectures. The proposed method reduces dynamic power dissipation significantly, simplifies design process for single and multiple output generation, and eliminates the need of some hardware [3].

Dhinesh. H, Adhiyaman. G, Esakki Muthu. A. et al. Low power dissipation is very

critical in today's electronic designs. Linear feedback shift registers are anefficient way of describing and generating certain sequences in hardware implementations. A linear feedback shift register composed of a shift register R which contains a sequence of bits and a feedback function F which is the bit sum (XOR) of the entries of the shift register. The performance on parallel architecture of LFSR reduces dynamic power consumption significantly, compared to the conventional architecture and showed the way to generate multiple outputs. The proposed method significantly reduces dynamic power dissipation, simplifies the design process for single and multiple output generation, and eliminate the need of some hardware. The achievable rate and power reduction to improve the performance in parallel architecture by implementing Integrated clock gating. The Integrated clock gating achieves substantial reduction on the power consumption by reducing the gate count and dynamic power dissipation [4].

III. METHODOLOGY

The proposed methodology begins with the design and implementation of a Built-In Self-Test (BIST) framework integrated into nanoscale devices for reliable fault detection. The architecture leverages the concept of parallelism to enhance the speed and efficiency of testing operations. A Linear Feedback Shift Register (LFSR) is used as the core test pattern generator (TPG) due to its simplicity, low hardware overhead, and ability to produce pseudo-random sequences. To achieve a high degree of fault coverage, the LFSR is configured in a parallel structure, enabling simultaneous generation of multiple test vectors rather than traditional serial bit-wise shifting.

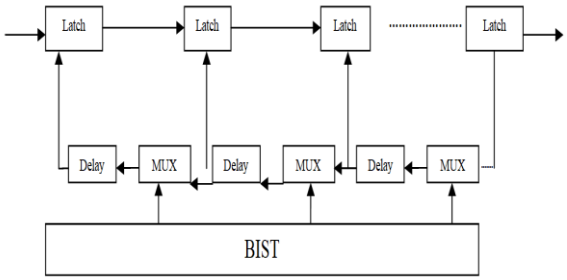

Fig. 1: Block Diagram

Next, the parallel LFSR architecture is developed with optimized feedback logic to maintain randomness while ensuring hardware efficiency. Polynomial selection plays a crucial role in maximizing the spread of generated test vectors. The parallel implementation is realized by partitioning the LFSR into sub-blocks that work all together, thereby reducing test time in comparison to conventional single-chain architectures. This design is synthesized and simulated using hardware description languages (HDL) to validate its correctness and assess timing performance.

To further improve test efficiency, scan chain optimization techniques are incorporated. Instead of using long, unoptimized scan chains that lead to redundant test cycles, the methodology focuses on reordering and balancing scan chains to minimize switching activity and power consumption. Parallel scan insertion ensures that the multiple test vectors generated by the LFSR are efficiently applied to the circuit under test (CUT),

thereby reducing test application time while maintaining structural fault coverage.

Additionally, the LFSR test vector modification strategies to overcome the limitations of purely random patterns. Weighted pattern generation and reseeding techniques are applied to increase the detection of random-pattern-resistant faults. By modifying the initial seed values and adjusting probability weights, the parallel LFSR can dynamically alter its output sequence to cover a broader fault spectrum. This adaptive approach ensures that the architecture is suitable for nanoscale devices, where defect density is higher and fault types are more complex.

Finally, the entire BIST-based parallel LFSR architecture is evaluated through simulation and synthesis on benchmark circuits. Performance metrics such as fault coverage, hardware overhead, power dissipation and test time are analyzed. Comparisons are made with traditional serial LFSR and conventional BIST methods to validate the effectiveness of the proposed approach. Experimental results are used to demonstrate that the methodology significantly enhances fault detection in nanoscale devices while maintaining design efficiency, thus providing a scalable and practical solution for future integrated circuit testing.

IV. RESULTS

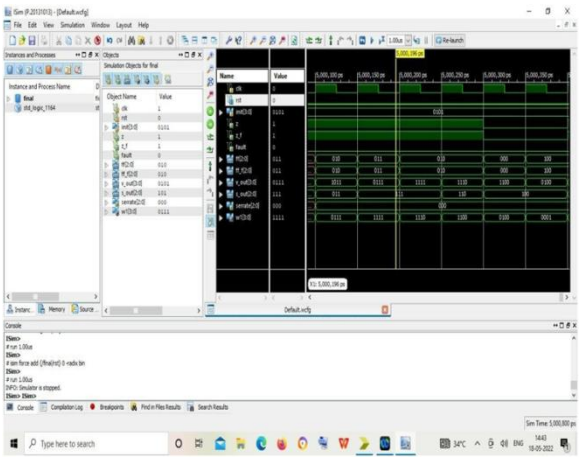

Fig. 2: Output without Fault

Figure 2 shows the simulation output of the parallel LFSR architecture under fault-free conditions, where the generated test vectors match the expected responses. The waveform confirms correct BIST operation with no errors detected in the circuit under test.

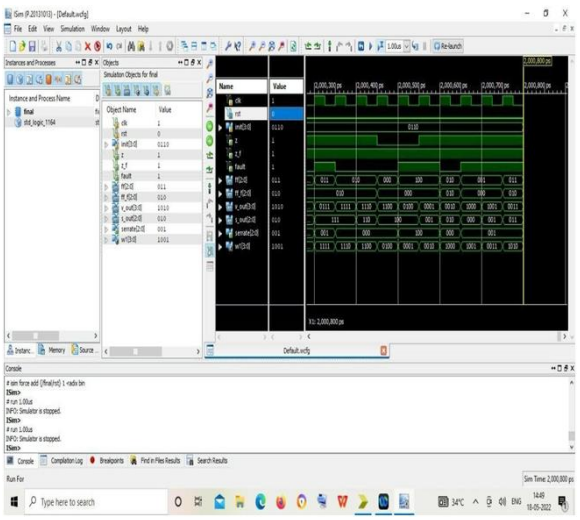

Fig. 3: Output with Fault

Figure 3 illustrates the simulation output of the parallel LFSR architecture under faulty conditions, where mismatches between expected and actual responses are

observed. The waveform confirms the effectiveness of the BIST in detecting faults within the circuit under test.

V. CONCLUSION

The proposed BIST-based parallel LFSR architecture effectively enhances test efficiency in nanoscale devices by combining scan chain optimization with modified test vector generation. The approach achieves higher fault coverage with reduced power consumption and test time, while maintaining low hardware overhead. Its scalability and adaptability make it a robust solution for VLSI testing, cryptographic security, and safety-critical applications, addressing the shortcomings of conventional testing methods in advanced integrated circuits.

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