# A CMOS FREQUENCY DIVIDER WITH LOW-POWER DYNAMIC TAIL CURRENT CONTROLLED CML LATCHES

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**ABSTRACT: An analysis of regenerative dividers predicts the required phase shift or selectivity for proper operation. Frequency divider circuits divide the frequency of an input signal by a specified ratio. They are critical components in analog, digital, and mixed-signal microelectronics. In power-constrained environments, such as cryogenic electronics or implanted biomedical devices, minimizing power consumption is crucial. Frequency synthesis and clock generation use Current-Mode Logic (CML) dividers because high-speed digital systems are depended on often. Because of continuous biased tail current, conventional CML dividers consume significant static power that considers input activity or frequency. Therefore, this issue is overcome by using this proposed dynamic biasing architecture that adaptively controls the tail current of CML latches based on real-time operational parameters such as input clock frequency or system activity. The proposed circuit integrates with three key components, such as a frequency/activity sensor (derived from a PLL control voltage or counter), adaptive control logic mapping frequency to bias levels, and a programmable current source (IDAC(Current Digital-to-Analog Converter)) that integrates with pulse-based gating of the tail path. Simulation results demonstrate that the divider achieves significant power savings at low-to-moderate frequencies for maintaining exact operation at high speeds and increase the transconductance (gm) when higher operating speeds are demanded. Thus, in modern PLL(Modern Phase-Locked Loops) and SerDes applications, the proposed architecture provides a scalable solution for low-power and high-speed frequency dividers.**

**KEYWORDS: Current-Mode Logic (CML) dividers, Programmable Current Source, transconductance (gm), Modern Phase-Locked Loops (PLLs), Tail Current**

## I. INTRODUCTION

Frequency dividers are fundamental auxiliary components in analog, digital, and mixed-signal microelectronic circuits, used in applications such as frequency synthesis, clock recovery, quadrature generation, and signal processing[1].

In applications where the thermal budget and/or the available energy limit power consumption, it is crucial for the frequency divider to dissipate as little power as possible. Frequency dividers as a part of cryogenic control electronics for qubits [2] or of biomedical implanted/wearable electronic devices are significant examples. A frequency divider can be designed by adopting different typologies, including Current Mode Logic (CML), Injection-Locking (IL), and True Single-Phase Clock (TSPC). Each of them offers unique trade-offs in terms of power consumption, speed, complexity, and robustness. Furthermore, their operational principles differ: the IL approach is purely analog, TSPC is purely digital, and CML is mixed-signal[3].

Each typology excels in distinct application areas. CML circuits can operate at very high speeds, making them suitable for high-frequency communication systems, such as transceivers [4], high-speed data links, and 5G wireless networks, with the future challenge of shifting toward 6G.

In particular, CML frequency dividers are adopted in Phase-Locked Loops (PLLs) and RF/microwave systems [5].

On the other hand, Injection-Locked Frequency Dividers (ILFDs) generate frequency-stable signals while consuming very low power. Thus, they are commonly used in low-power biomedical devices, such as implantable devices [6], where energy efficiency is critical to prolong battery life. They are also used for low-power wireless communication applications, such as CML frequency dividers.

Finally, TSPC frequency dividers are easy to integrate, occupy a small silicon area, and consume low power. They are used in digital signal processing systems, including radar and image and sound transmission systems [7]. Additionally, they are key components in high-performance computing systems, such as CPUs, GPUs, and FPGAs. Furthermore, TSPC frequency dividers are employed in high-frequency communication systems, such as PLLs for RF circuits [8].

High performance logic circuits having low-power and high data rate have emerged due to the increasing demand for high-speed communication, namely, SerDes [9]. High noise immunity and clock rates are also essential for the basic building blocks. The most important building block of a SerDes is a latch, where CML is preferred to meet the power requirements. the use of several stacked gates in a CMOS and makes conventional circuits unsuitable [10]. Further, short channel effects degrade small-signal parameters and limit the use of CMOS in sub nanometer era. This affects the intrinsic gain of the gates and degrades noise margin. Even though novel CML circuits have been presented, the problem of stacking several level of gates under a low voltage constraint has not been discussed. Novel approaches accommodate additional gates to operate at low Vdd and high-speed. These gates require bias circuitry, which results in a complex design and increases layout area. In a given process and Vdd, latches using CML logic are established in terms of Pavg, td, figure of merit (FoM), power delay product (PDP) and output noise. It is imperative for a latch to provide delay time intervals with varying offset for a specific application even under identical biasing conditions. This happens due to process, voltage and temperature (PVT). In a SerDes other circuits are included along with latch while connected to a common VP and all do not operate at the same time. As some circuits are suddenly turned on, an abrupt current is drawn. VP droops and oscillates with time due to Ldi/dt noise. It is imperative to understand the effect of power supply noise (PSN) on delay and how the jitter so introduced varies with PSN[11].

Phase-locked loop (PLL)-type frequency synthesizers are widely used to generate local frequency signals in RF transceivers. Programmable frequency dividers are indispensable in PLL-type frequency synthesizers[12]. Important specifications, such as a wide operation frequency range, low phase noise, and low power consumption are significant to programmable frequency dividers[13]. Frequency dividers on the basis of a fixed-modulus divider chain are introduced to frequency synthesizers to achieve a higher operating frequency and a wider frequency range. Nevertheless, the frequency divider is not able to work with any different frequency division ratio because the frequency division ratio is fixed by the PLL system in this case[14].

Frequency dividers are crucial circuits that are employed in PLLs and high-speed serializers/deserializers (serdes). Frequency dividers fall under three categories: (1) flip-flop-based frequency dividers, (2) injection-locked frequency dividers, and (3) regenerative frequency dividers. Injection-locked frequency dividers employ an oscillator whose center frequency is locked to a harmonic of the incoming signal frequency[15]. The input signal is injected through a voltage node of the oscillator. While achieving low-power operation, injection-locked frequency dividers exhibit a narrow lock-range. Regenerative frequency dividers, first introduced and realized by placing a mixer and a low-pass filter in a closed-loop feedback. A regenerative frequency divider exhibits a wider lock range at very high frequencies compared to an injection-locked counterpart, but utilizes many passive components in the process. Since

frequency dividers are ubiquitous in modern high-speed systems, the excessive use of passive components is a disadvantage from overall chip-area and circuit matching considerations.

## II. LITERATURE SURVEY

T. Baluta, A. Meyer, A. Dossanov, Y. Kudabay, L. Bakhchova and V. Issakov, et al. [16] presents a low-power frequency divider chain with a division ratio of 2048 realized in a 22nm FDSOI CMOS technology. To optimize the power consumption, yet achieve high-speed operation, we realize the first stages using the CML logic, while the subsequent stages are implemented in TSPC logic and finally, the lower speed stages use the classical CMOS logic. Thus, we achieve an optimally low power consumption as we advance along the frequency divider chain from 22GHz at the input down to 10.74MHz at the output. The entire chain dissipates only 8.75mA from a single 0.8V supply, distributed as follows: the active balun at the input consumes 4 mA, while the frequency divider chain itself draws only 4.75 mA. The chip is inductorless and thus very compact. The presented chip occupies a minimal area of only 510 by 360 μm including pads.

H. -E. Liu, W. -C. Chen and H. -Y. Chang, et al. [17] a W-band quadrature voltage-controlled oscillator (QVCO) with an injection-locked frequency divider (ILFD) is presented using 40-nm CMOS process. The QVCO is designed using a modified self-injection topology to minimize the quadrature error and phase noise. The injection-locked technique is employed in the frequency divider to achieve high frequency with low dc power consumption, and the division ratio is 3. The measured tuning range of the QVCO is from 93.3 to 97.4 GHz with a single-end output power of higher than -24 dBm. The measured average free-running phase noise of the QVCO is -80 dBc/Hz at 1-MHz offset. The overall dc power consumption of the QVCO and ILFD is 43 mW. The presented circuits are suitable for the phase-locked loop frontend.

H. Nam and J. -D. Park, et al. [18] compact W-band divide-by-three injection-locked frequency divider (ILFD) is presented in 65-nm CMOS technology. To provide a wide locking range, we propose inductive feedback to boost the injection current. With the proposed approach, the locking range of the ILFD can be wider than 10% without any varactor and additional power dissipation which is more than three times the locking range compared with the reference ILFD without boosting of the current injection. The measured locking range of the proposed ILFD was from 73.9 to 82.5 GHz with the W-band input signal power of 0 dBm, and the phase noise at 1 MHz was -117.13 dBc/Hz at the input frequency of 78 GHz. The implemented ILFD with the inductive feedback consumes 7.88 mW under a 1 V supply, and its core size is 0.22 $mm^2$.

A. Patnaik and D. Yoon, et al. [19] presents a divide-by-2 static current-mode logic (CML) frequency divider with inductive peaking. While inductive peaking frequency dividers feature a high-Q resonator that limits the operation range, a frequency tuning technique has been implemented to extend the operation range. An nMOS transistor pair has been employed at the source of the cross-coupled pair to adjust the current flow and output node capacitance, thereby modifying the frequency divider's operation range. Fabricated in 90-nm CMOS, the frequency divider occupies a core chip area of 170×240 μ m2 and achieves an operation range of 90.9% (24–64 GHz). It dissipates a maximum dc power of 30.1 mW from a 1.2 V supply voltage.

Z. Tibenszky, C. Carta and F. Ellinger, et al.[20] presents a divide-by-4 TSPC frequency divider operating with supply

voltages from 0.4 V to 0.9 V and covering input frequency ranges from below 100 MHz to 70 GHz and beyond. The operating frequency and the required input power is adjustable through the backgate voltages of the transistors of the employed fully depleted silicon on insulator (FD-SOI) technology. When operating at 70 GHz, the divider core consumes only 393 mA from a 0.9 V supply, which correspond to a FoM of 195 GHz/mW. To the best knowledge of the authors, the presented circuit demonstrates the highest reported operating frequency for TSPC dividers, and smallest area and lowest current consumption values among RF frequency dividers reported to date.

H. -Y. Chang, W. -C. Chen, H. -N. Yeh and I. Y. -E. Shen, et al. [21] presents V-band low-dc-power wide-locking-range divideby-6 injection-locked frequency divider (ILFD) using a 90-nm CMOS process is proposed in this letter. The proposed innovative topology is composed of current-reused oscillation cores with transformer coupling. Moreover, the dc bias of the injectors can be properly applied to widen the locking range (LR). With a core dc power of 5.6 mW and an input power of -5 dBm, the measured maximum locking is 5.6 GHz (9.8%) from 54.5 to 60.1 GHz. When compared to the previously reported V-band ILFDs, this work features a high division ratio, low dc power, wide LR, and good sensitivity.

U. -G. Choi and J. -R. Yang, et al. [22] proposes CMOS two-way differential power divider is proposed to reduce the insertion loss (IL) and size in the D -band. The power distribution is achieved using a low-loss differential power divider with a capacitive loading structure, without modifying the matching network of the unit devices. In addition, the degradation of the IL due to the parasitic inductance of groundings is made negligible by using the virtual ground of the differential structure. The impedance of the differential-mode transmission line (TL), which is half that of the single-ended line, is designed in the impedance range achievable in the bulk CMOS process, utilizing capacitive loading techniques. The 3-D electromagnetic (EM) simulation results of a two-way power divider show a low IL within 0.35 dB at 110–170 GHz. The proposed power divider achieves a measured minimum IL of 0.32 dB at 160 GHz with a core size of 0.0075 mm2.

Y. Geng, H. Lin, B. Wang and C. Wang, et al.[23] Main-stream quantum computers employ dispersive reflectometry for quantum-bit (Qubit) state discrimination. An all-parametric quantum reflectometer (APQR) scheme has been proposed for high-fidelity, scalable Qubit array readout in this letter. For the RF excitation of APQR, a 10.7–16.9 GHz 65-nm cryogenic CMOS (Cryo-CMOS) parametric frequency divider (PFD) is demonstrated here. It adopts a pair of parallelly connected nonlinear artificial transmission lines (NLATLs), a wideband varactor-based dynamic coupler, and a transformer-based CM filter (TCMF). Due to the minimized device self-heating without dc power consumption and the intrinsic common-mode (CM) to differential-mode (DM) isolation, the PFD presents a measured output thermal noise floor of −189.1 dBm/Hz at 4.2 K. This is only 3.3 dB higher than 4.2-K blackbody radiation. At 4.2 K, the PFD also exhibits an ultralow phase noise of −128.8 dBc/Hz at 1 MHz at 6.75 GHz, which is 2.6 dB lower than a conventional Cryo-CMOS CML divider. It presents a 44.9% relative bandwidth at 4.2 K, which is 2× of the prior art at 300 K.

T. H. Cheung, J. Ryynänen, A. Pärssinen and K. Stadius, et al. [24] describes the design and post-layout simulations of a 2/3/4- modulus frequency divider circuit, accompanied with an accumulator that controls the division count. The circuit is capable of operating as an integer or as a

fractional divider. Key topic of this paper is the merging of div-2/3 and div-3/4 circuits into a single compact circuit that solves an issue of a forbidden state in fractional-division operation. The circuit is designed with 28-nm CMOS technology and the post-layout simulations indicate an operating input frequency range of 0.3 - 5.4 GHz with 13-bit fractional frequency resolution between division ratios of 2-4. The divider occupies only 40 pm × 30 pm while consuming 2.0 mW at 5.4 GHz input frequency.

M. Yan, H. M. E. Hussein, C. Cassella, M. Rinaldi and M. Onabajo, et. al [25] presents a CMOS 2:1 differential parametric frequency divider (PFD) design with an output frequency of 2.4 GHz and an input voltage range of 450~890 mV at 4.8 GHz. The topology is suitable for integration into RF Systems-on-a-Chip (SoCs), and has been constructed for sub-6 GHz applications. A design and optimization methodology for this on-chip PFD is also described in this paper. The simulation results show a performance improvement of the proposed differential PFD compared to a single-ended PFD designed for the same output frequency in the same 65nm CMOS technology.

## III. FRAMEWORK A CMOS FREQUENCY DIVIDER WITH LOW-POWER DYNAMIC TAIL CURRENT CONTROLLED CML LATCHES

In this section, a framework a CMOS frequency divider with low-power dynamic tail current controlled CML latches is observed in figure 1. This process initially starts with the input signal or input clock frequency (Fin) or internal divider activity. The real-time operational parameter indicates how fast the divider is working because at higher Fin. The latch needs more tail current to switch fast and reliably at lower Fin. This can use less current to save power. A PLL tap (control voltage proportional to frequency) or a comparator/counter can be used. The current operating speed of the system is represented by frequency code or analog voltage and “feedback mechanism” is mentioned in your proposal. Control Logic for sensor output goes to a control block that decides current the latch really needs.

Example:

If Fin is high → set tail current high.

If Fin is medium → set tail current moderate.

If Fin is low/idle → set tail current low or off.

This ensures minimum power is used without losing speed.

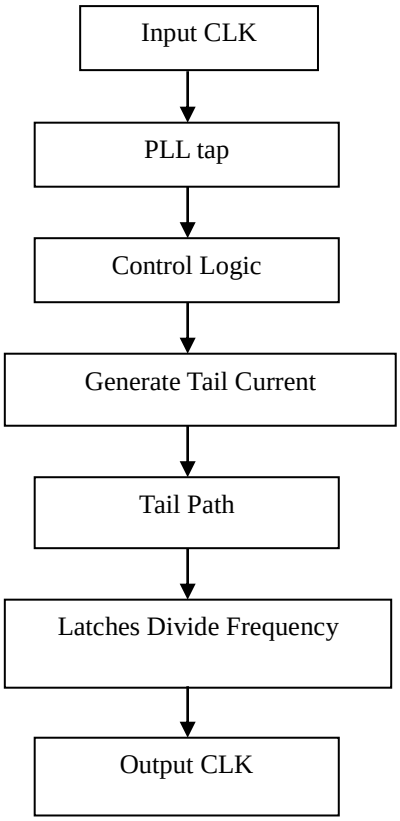


**Figure.1: Framework a CMOS Frequency Divider with Low-Power Dynamic Tail Current Controlled CML Latches**

IDAC (Digital-to-Analog Current Source) will control block drives an IDAC (current-steering DAC) and generates the required tail current (I_tail) that will bias

the CML latches. In conventional dividers, current is programmable and adaptive, unlike a fixed current source. Enable Pulse Generator of an edge detector and one-shot circuit creates a narrow enable pulse (ΦE) at each clock edge. This pulse turns ON the tail transistor only during evaluation (sampling moment) for rest of the time for tail current is OFF, further saving power. CML Latches (Master–Slave Divider Core) for master–slave CML latches perform the actual divide-by-2 operation that consumes current. The enable pulse (ΦE) is active and IDAC has set the required tail current level and frequency-divided signal at Qout with much lower average power consumption. The sensor updates the control logic, which reprograms the IDAC and pulse width dynamically as input conditions changes. In real time. low-power, adapting and fast in closed loop.

In digital circuits, Input CLK refers to a clock signal that acts as a timing reference. It's a periodic signal that synchronizes the operations of various components within the circuit, ensuring that data is processed and transferred at the correct time. Think of it as the "heartbeat" of the circuit, dictating when actions should occur. The inputs are the data (D) input and a clock (CLK) input. The clock is a timing pulse generated by the equipment to control operations. The D flip-flop is used to store data at a predetermined time and hold it until it is needed.

In a phase-locked loop (PLL), a "tap" generally refers to a specific point or stage within the feedback loop, often associated with a filter or delay element, that influences the loop's behavior. These taps can be used to adjust the loop's response to input signals, affecting its stability, lock time, and ability to track frequency or phase changes. taps in a PLL are strategically placed points in the feedback loop that allow for fine-tuning and optimization of the loop's behavior. They are crucial for achieving stability, fast lock times, and low jitter in various applications. According to multiple electronics resources, PLLs are a fundamental building block in radio, wireless, and telecommunications systems.

Control logic is the set of rules and instructions that govern how a system responds to inputs, events, and conditions to achieve a desired outcome or maintain specific conditions. It's essentially the "brain" behind a system's automated behavior, determining what actions to take based on the situation. Control logic is defined as the detailed information about processes within a system, including the tagnames used in program logic, signals, PID control parameters, and various operating modes, enabling clear implementation of intended monitor and control functions. The tail current is made large when the oscillator output voltage reaches its maximum or minimum value and when the sensitivity of the output phase to injected noise is the smallest; the tail current is made small during the zero crossings of the output voltage when the phase noise sensitivity is large. The battery is considered as fully charged once the charge current has dropped to less than this “Tail current” parameter. The “Tail current” parameter is expressed as a percentage of the battery capacity.

A latch can function as a frequency divider by utilizing its ability to toggle its output state with each clock pulse. Specifically, connecting the inverted output (Q-bar) back to the input (D) of a D-latch effectively creates a divide-by-two circuit. Each clock cycle causes the latch to switch states, resulting in an output frequency that is half the input frequency. In digital electronics, Output CLK refers to the clock signal that is generated by a circuit or module and is used to synchronize the operations of other components within a system. It acts as a timing reference, ensuring that different parts of a circuit or

system work together in a coordinated manner. A clock signal is a periodic waveform, typically a square wave, that alternates between high and low voltage levels.

## IV. RESULT ANALYSIS

In this section, result analysis a CMOS frequency divider with low-power dynamic tail current controlled CML latches is observed.

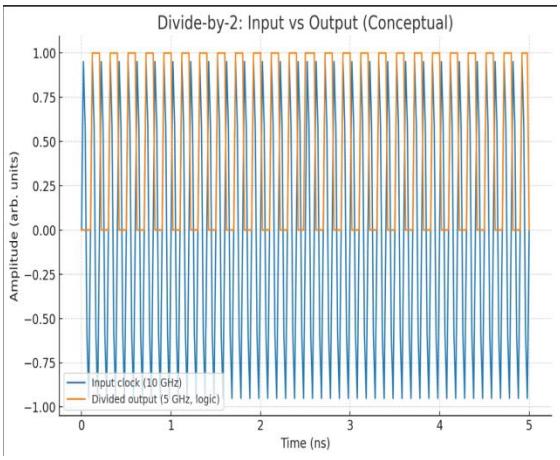


**Figure.2: Output**

The blue signal is the input clock running at 10 GHz and orange signal is the output of the divider, which runs at half the frequency (5 GHz). The output changes its state once for every two input cycles. This circuit is working as a divide-by-2 frequency divider.

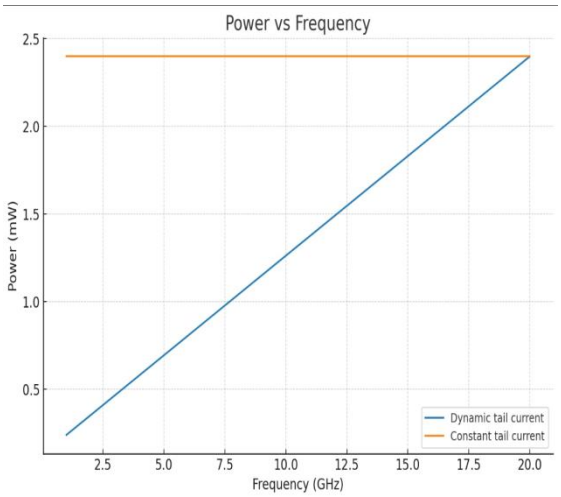


**Figure.3: Power Vs Frequency**

Orange line (Constant tail current) indicates Flat line, always around 2.4 mW and power consumption stays the same of operating frequency.

## V. CONCLUSION

In this section, CMOS frequency divider with low-power dynamic tail current controlled CML latches is concluded. The divider adaptively modulates its current consumption in real-time frequency sensing, digital control logic, and a programmable bias source, striking a balance between high-speed performance and energy efficiency. The proposed design activates its tail path only during short evaluation intervals, leading to substantial static power reduction without compromising signal integrity for unlike conventional static CML architectures. During idle periods, integration of common-mode feedback further stabilizes operation. The activity-aware biasing can extend the scalability of CML dividers to energy-constrained systems, making them highly suitable for next-generation high-speed, low-power PLLs, SerDes, and clock distribution networks demonstrated in this proposed system. Future work will focus on optimization of IDAC resolution, silicon implementation and exploring cross-stage sharing of adaptive bias resources.

## VI. REFERENCES

1. Peng, Y.; Benserhir, J.; Zou, Y.; Charbon, E. A Cryogenic Double-IF SSB Controller with Image Suppression and On-Chip Filtering Implemented in 130 nm SiGe BiCMOS Technology for Superconducting Qubit Control. In Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), Denver, CO, USA, 21–24 April 2024; pp. 1–2, doi:10.1109/CICC60959.2024.10528967

2. Badiali, A.; Borgarino, M. Cryo-CMOS Multi-Frequency Modulator for 2-Qubit Controller. Electronics 2024, 13, 2546.

https://doi.org/10.3390/electronics13132546
3. Lai, W.-C.; Jang, S.-L.; Li, C.-L. A Dual Band Divide-by-Four Frequency Divider for Biomedical Sensor and Wearable Applications. In Proceedings of the International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), Taipei, Taiwan, 26–28 October 2016; pp. 259–261.
4. Grewal, S.; Shah, O.A. Design and Analysis of High-Performance Frequency Divider in 32 nm CMOS Technology for Biomedical Applications. Int. J. Online Biomed. Eng. (Ijoe) 2023, 19, 69–87. DOI:10.3991/ijoe.v19i07.39145
5. Matig-a, G.E.; Yuce, M.R.; Redouté, J.-M. Design of a CML Transceiver with Self-Immunity to EMI in 0.18-µm CMOS. IEEE Trans. Circuits Syst. I Regul. Pap. 2017, 64, 981–991.
6. Casper, Bryan & O'Mahony, Frank. (2009). Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links—A Tutorial. Circuits and Systems I: Regular Papers, IEEE Transactions on. 56. 17 - 39. 10.1109/TCSI.2008.931647..
7. Waks, Adam & Tesson, O. & Bellanger, Mike & Taris, T. & Begueret, Jean-Baptiste. (2022). Design of a 5G Application CML Frequency Divider for Improved Efficiency. 21-24. 10.23919/EuMIC54520.2022.9923472.
8. Wang, D.; Bazzi, A.; Chafii, M. RIS-Enabled Integrated Sensing and Communication for 6G Systems. In Proceedings of the IEEE Wireless Communications and Networking Conference (WCNC), Dubai, United Arab Emirates, 21–24 April 2024; pp. 1–6. https://doi.org/10.48550/arXiv.2401.00444
9. Wang, Y.; Liu, Y.; Xu, H.; Li, Z.; Li, Z. A Wideband and Low Reference Spur PLL with Clock Feedthrough Suppressed and Low Current Mismatch Charge Pump and Symmetrical CML Divider. Electronics 2023, 12, 4164. https://doi.org/10.3390/electronics12194164
10. A. Ghilioni, A. Mazzanti and F. Svelto, "Analysis and Design of mm-Wave Frequency Dividers Based on Dynamic Latches With Load Modulation," in IEEE Journal of Solid-State Circuits, vol. 48, no. 8, pp. 1842-1850, Aug. 2013, doi: 10.1109/JSSC.2013.2258793
11. Junliang Wang, Zhigong Wang, Jian Xu, Yiqiang Wu, Mi Tian, Xuemei Lei, Li Ma, and Lu Tang. 2014. A multi-band CMOS PLL-based frequency synthesizer for DRM/DRM+/DAB systems. Analog Integr. Circuits Signal Process. 80, 2 (August 2014), 293–304. https://doi.org/10.1007/s10470-014-0341-x
12. Huang, Z.; Luong, H.C. Z. Huang and H. C. Luong, "An 82–107.6-GHz Integer- N ADPLL Employing a DCO With Split Transformer and Dual-Path Switched-Capacitor Ladder and a Clock-Skew-Sampling Delta–Sigma TDC," in IEEE Journal of Solid-State Circuits, vol. 54, no. 2, pp. 358-367, Feb. 2019, doi: 10.1109/JSSC.2018.2876462.
13. S. Huang, S. Liu, J. Hu, R. Wang and Z. Zhu, "A 12-GHz Wideband Fractional-N PLL With Robust VCO in 65-nm CMOS," in IEEE Microwave and Wireless Components Letters, vol. 29, no. 6, pp. 397-399, June 2019, doi: 10.1109/LMWC.2019.2909656.
14. Delden, M.v.; Pohl, N.; Aufinger, K.; Musch, T. A 94 GHz programmable frequency divider with inductive peaking for wideband and highly stable frequency synthesizers. In Proceedings of the 2017 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, Germany, 8–10 October 2017; pp. 9–12, doi:10.23919/EuMIC.2017.8230647
15. Issakov, V.; Trotta, S. Low-power dual-modulus frequency divider by 4/5 up to 13-GHz in 0.13 µm CMOS. In Proceedings of the 2017 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), Tel-Aviv, Israel, 13–

15 November 2017; pp. 1–4, doi: 10.1109/COMCAS.2017.8244784.
16. T. Baluta, A. Meyer, A. Dossanov, Y. Kudabay, L. Bakhchova and V. Issakov, "A 7mW 22 GHz Frequency Divider Chain by 2048 using CML, TSPC and CMOS Logic in 22FDX," *2025 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, San Juan, PR, USA, 2025, pp. 42-45, doi: 10.1109/SiRF63957.2025.11076818.
17. H. -E. Liu, W. -C. Chen and H. -Y. Chang, "A W-band Quadrature Voltage-Controlled Oscillator with an Injection-Locked Frequency Divider in 40-nm CMOS Process," *2021 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, Hualien, Taiwan, 2021, pp. 1-3, doi: 10.1109/RFIT52905.2021.9565268.
18. H. Nam and J. -D. Park, "A W-Band Divide-by-Three Injection-Locked Frequency Divider With Injection Current Boosting Utilizing Inductive Feedback in 65-nm CMOS," in *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 5, pp. 516-519, May 2020, doi: 10.1109/LMWC.2020.2983014.
19. A. Patnaik and D. Yoon, "A 24–64 GHz Wideband Static CML Frequency Divider in a 90-nm CMOS Technology," in *IEEE Microwave and Wireless Technology Letters*, vol. 35, no. 1, pp. 71-74, Jan. 2025, doi: 10.1109/LMWT.2024.3479166.
20. Z. Tibenszky, C. Carta and F. Ellinger, "A 0.35 mW 70 GHz Divide-by-4 TSPC Frequency Divider on 22 nm FD-SOI CMOS Technology," *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Los Angeles, CA, USA, 2020, pp. 243-246, doi: 10.1109/RFIC49505.2020.9218362.
21. H. -Y. Chang, W. -C. Chen, H. -N. Yeh and I. Y. -E. Shen, "A V-Band CMOS Low-DC-Power Wide-Locking-Range Divide-by-6 Injection-Locked Frequency Divider Using Transformer Coupling," in *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 6, pp. 593-596, June 2020, doi: 10.1109/LMWC.2020.2992107.
22. U. -G. Choi and J. -R. Yang, "A D-Band Two-Way Differential Power Divider on 65-nm CMOS Process," in *IEEE Microwave and Wireless Technology Letters*, vol. 34, no. 3, pp. 279-282, March 2024, doi: 10.1109/LMWT.2024.3353483.
23. Y. Geng, H. Lin, B. Wang and C. Wang, "A Cryo-CMOS Parametric Frequency Divider With −189.1 dBm/Hz Output Noise Floor at 4.2 K for High-Fidelity All-Parametric Quantum Reflectometer," in *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 12, pp. 1650-1653, Dec. 2023, doi: 10.1109/LMWT.2023.3325730.
24. T. H. Cheung, J. Ryynänen, A. Pärssinen and K. Stadius, "A 5.4-GHz 2/3/4-Modulus Fractional Frequency Divider Circuit in 28-nm CMOS," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401405.
25. M. Yan, H. M. E. Hussein, C. Cassella, M. Rinaldi and M. Onabajo, "Design of a CMOS Parametric Frequency Divider with 2.4-GHz Output Frequency for RF Systems-on-a-Chip," *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, Austin, TX, USA, 2022, pp. 1978-1982, doi: 10.1109/ISCAS48785.2022.9937745.