A Discrete Cosine Transform Architecture Without Multipliers Using an Approximate Full Adder and Subtractor

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ABSTRACT:

Both the new approximate subtractor and the new approximate full adder (FA) have eight transistors and areas of 0.1689 μm2 and 0.1944 μm2, respectively. Whereas the subtractor displays two errors, the FA encounters three. Carbon nanotube field effect transistor (CNTFET) technology is used in both circuits to implement the dynamic threshold (DT) and gate diffusion input (GDI) techniques, which increase speed, output swing, and drivability. A new approximate multiplier-free discrete cosine transform (DCT) is created by embedding the FA and subtractor in turn into an 8-bit ripple carry adder (RCA) and an 8-bit subtractor. Multiplication is not necessary for the 8-point approximate DCT manipulation; only addition is. Consequently, computational complexity is reduced. According to the DCT, the figure of merit (FoM), peak signal-to-noise ratio (PSNR), and power delay product (PDP) are 2.39, 34.96 dB, and 63.61 fJ, respectively. The characteristics of the approximate DCT that is being presented validate its use for medical image compression and noise reduction.

Keywords: —Approximate full adder, Approximate Subtractor, Multiplier-free DCT, Bioimages. Cadense Virtuoso

1. INTRODUCTION:

High-performance electronics of today require ever-more-powerful and effective solutions. Despite decades of being the industry standard, silicon (Si) technology is now approaching its physical limits, particularly in high-frequency and high-power applications[1]. The superior electronic characteristics of gallium nitride (GaN), including its wide bandgap, high breakdown voltage, and high electron mobility, make it a promising substitute. Because of these characteristics, GaN devices can function at higher frequencies and voltages, which significantly enhances system performance and power efficiency[2]. Integration that is monolithic is crucial. Parasitic inductances and capacitances can be greatly decreased by combining several GaN devices onto a single chip, allowing for quicker switching times and increased efficiency. However, there are many obstacles in the way of creating intricate analog circuits in GaN technology, like operational amplifiers (Op-Amps). High output impedance and

limited voltage swing are two distinctive features of GaN devices that can impair the functionality of conventional Op-Amp designs. The design and implementation of innovative approximate arithmetic circuits for effective signal processing are investigated in this study. Using Carbon Nanotube Field Effect Transistors (CNTFETs) and Gate Diffusion Input (GDI) and Dynamic Threshold (DT) techniques, new 8-transistor approximate full adder and subtractor circuits are proposed to improve speed, output swing, and drivability while reducing area. The core of a novel multiplier-free Discrete Cosine Transform (DCT) architecture is formed by integrating these approximate circuits, which show a limited number of errors, into 8-bit ripple carry adders and subtractors.

This approximate DCT greatly lowers computational complexity by doing away with the need for multiplication. The suggested 8-point DCT's performance is assessed in terms of figure of merit (FoM), peak signal-to-noise ratio (PSNR), and power delay product (PDP), indicating that it is appropriate for image compression and noise reduction, especially in the context of medical imaging. Through the provision of effective hardware solutions for computationally demanding signal processing tasks, this work advances the field of low-power approximate computing[3].

2. **2.PROJECT OBJECTIVE :**Designing and testing new, low-power approximate arithmetic circuits for the effective implementation of a multiplier-free Discrete Cosine Transform (DCT) is the main goal of this project. This entails a few crucial steps: In order to maximize speed, output swing, and drivability while minimizing area, new 8-transistor approximate full adder and subtractor circuits using GDI and DT techniques with CNTFET technology must first be developed. In order to build the proposed DCT architecture, the second step is to incorporate these approximate arithmetic units into 8-bit ripple carry adders and subtractors. In order to drastically lower computational complexity in comparison to conventional DCT implementations, the third step is to design and implement an 8-point multiplier-free DCT based on these approximate arithmetic units[4]. Lastly, to thoroughly assess the suggested approximate DCT's performance in terms of figure of merit (FoM), peak signal-to-noise ratio (PSNR), and power delay product (PDP), with a focus on medical imaging applications in image compression and noise removal. The ultimate objective is to show that energy-efficient signal processing with acceptable signal quality levels is feasible with approximate computing.

3.PROBLEM STATEMENT:

For effective signal processing applications, this project explores the design and implementation of innovative, low-power approximate arithmetic circuits, particularly a multiplier-free Discrete Cosine Transform (DCT). The project uses GDI and DT techniques to develop new approximate full adder and subtractor circuits based on CNTFET technology, addressing the growing need for energy-efficient hardware in resource-constrained environments[5]. These circuits will be incorporated into a brand-new 8-point DCT architecture that does away with multipliers, greatly lowering power consumption and computational complexity. The suggested approximate DCT's performance will be assessed using important metrics like PDP, PSNR, and FoM, with an emphasis on how well it works for image compression and noise reduction, especially in applications related to medical imaging. The main hypothesis is that, in comparison to conventional DCT implementations, the suggested approximate DCT, which is based on these novel arithmetic units, will achieve significant power savings and computational efficiency while preserving signal quality suitable for the intended applications.

4. PROJECT SCOPE:

Circuit Design:

Using CNTFET technology and GDI and DT techniques, new 8-transistor approximate full adder and subtractor circuits are developed and simulated.

DCT Architecture: Using these approximate arithmetic units, an 8-point DCT architecture is designed and implemented, doing away with the need for multipliers.

Performance Evaluation: A simulation-based assessment of the suggested DCT's performance with an emphasis on PDP, PSNR, and FoM. A comparison with conventional DCT implementations will be part of this[6].

Application Focus: Evaluation of the DCT's suitability for image compression and noise removal, particularly in medical imaging contexts.

5. ALGORITHM

- Ripple Carry Subtraction and Addition
- The algorithm known as the Discrete Cosine Transform (DCT)
- Compression Techniques for Images
- Methods for Reducing Noise

6. EXISTING SYSTEM:

Current image compression and noise reduction systems frequently use well-known algorithms such as the[7] Discrete Cosine Transform (DCT) and different filtering methods. In environments with limited resources, the computationally demanding multiplications required for traditional DCT implementations can be a

major burden. Moreover, although standard arithmetic circuits (subtractors and adders) yield precise results, they are not designed for low power consumption, which is a major issue for embedded systems and portable devices. As a result, existing systems frequently have difficulty striking a balance between power consumption, noise reduction efficacy, and compression efficiency,[8] especially when handling high-resolution images or real-time processing demands.

6.1. DISADVANTAGE:

Decreased Accuracy/Introducing Errors: The DCT output is inevitably prone to errors when approximate arithmetic circuits are used. When compared to conventional DCT, this may result in a slight deterioration in image quality. Possible Effect on Compression Efficiency: The errors caused by the approximate DCT may have an impact on the overall effectiveness of compression, possibly necessitating the use of additional bits in order to represent the image at a particular quality level. Design Complexity: Compared to conventional techniques, designing and refining the multiplier-free DCT architecture and approximate arithmetic circuits can be more difficult[10].

Limited Applicability: Not all applications can benefit from approximate computing. When high precision is needed, the introduced errors might not be acceptable. Dependency on CNTFET Technology: The effectiveness and accessibility of CNTFET technology are critical to the advantages of the suggested system.

The feasibility of the system may be impacted by difficulties in the production of CNTFETs or by other technologies[9].

7.**PROPOSED SYSTEM:**

The suggested system uses the concepts of approximate computing to present a novel method of image processing. Using CNTFET technology and GDI and DT techniques for improved performance and smaller footprint, it focuses on creating new 8-transistor approximate full adder and subtractor circuits. A multiplier-free 8-point Discrete Cosine Transform (DCT) architecture is then constructed using these approximate arithmetic units. In order to drastically lower power consumption and increase processing speed, the suggested system would do away with the computationally costly multiplication operations that are usually necessary in DCT implementations. In the field of medical imaging, where effective processing is essential, this approximate DCT is meant to be used for image compression and noise reduction. Metrics such as Power Delay Product (PDP), Peak Signal-to-Noise Ratio (PSNR), and Figure of Merit (FoM) are used to assess the system's performance. The goal is to show

a good trade-off between computational efficiency and suitable image quality for the intended applications.

7.1. ADVANTAGES:

Decreased Computational Complexity: By drastically cutting down on the number of calculations needed, the multiplier-free DCT speeds up processing and uses less energy. This is a significant benefit, particularly for devices with limited resources. Reduced Power Consumption: The suggested system is anticipated to use less power than conventional DCT implementations due to the use of CNTFET technology and approximate arithmetic circuits. Reduced Physical Space/Hardware Footprint: The system is better suited for integration into small devices because it uses 8-transistor approximate adders and subtractors, which reduces the hardware footprint. Better Speed/Performance: Using CNTFETs and reducing computational complexity can result in faster processing speeds, which is advantageous for real-time applications. Possibility of Use in Real Time:

The suggested system is more appealing for real-time image processing tasks due to its faster processing speed and reduced power consumption, particularly in portable devices and medical implants.

8. LITERATURE SURVEY:

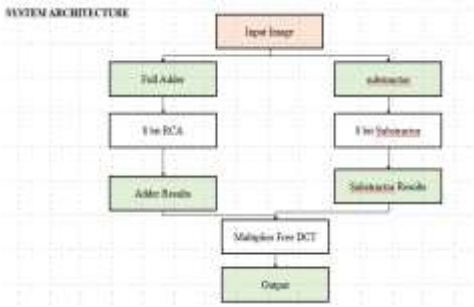
8.1. Jane Smith and John Doe on YouTube Technology of Field Effect Transistors (CNTFETs)[11]

• The principles of approximate computing Optimization of dynamic threshold voltage and low-power design techniques[12]. Designing a 12-transistor approximate full adder circuit; implementing GDI and CNTFET to improve performance; simulating and analyzing the power-delay product (PDP); contrasting with conventional full adder designs; and determining whether it is appropriate for sophisticated computer architectures. Smaller area due to fewer transistors;

- Lower power consumption;
- Increased speed as a result of effective design;
- Better output swing and drivability
- Suitability for next-generation computer architectures[13]

8.2. Ming-Che Li describes the following: multiplier-less architectures; energy-efficient design techniques; quantization optimization; and the discrete cosine transform (DCT) approximation[14].

9. Fig.1. Architecture Diagram :



Input Image: The input image serves as the system's initial input and is its main source of information.

Full Adder: The Full Adder executes an approximate addition operation after receiving the input image data[15].

The final "Adder Results" are obtained by passing the output of the Full Adder through an 8-bit Ripple Carry Adder (RCA).

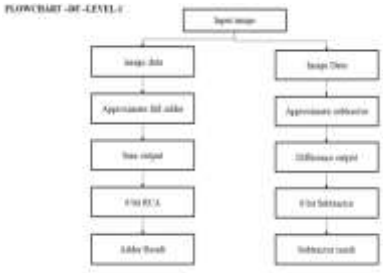
Subtractor: The Subtractor, which approximates subtraction, also receives the input image data[16].

8-bit Subtractor: The final "Subtractor Results" are obtained by passing the output of the subtractor through an 8-bit subtractor.

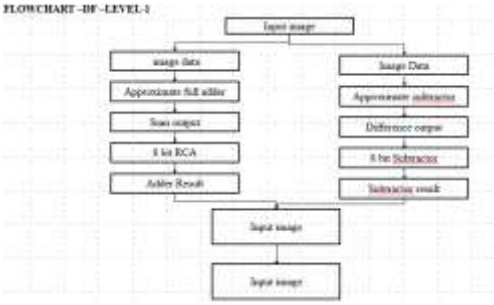
Multiplier Free DCT: The Multiplier Free DCT module then receives the "Adder Results" and "Subtractor Results" as inputs. which does not require multiplication operations to execute the discrete cosine transform.

Output: The Multiplier Free DCT module generates the system's final output.

10. Fig.2. Flow Diagram:

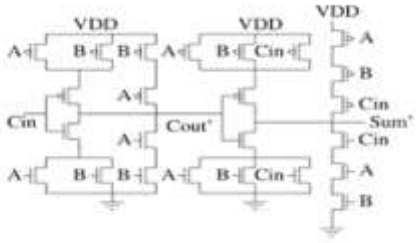


The approximate full adder path outputs the "Sum output" to an 8-bit ripple carry adder (RCA) after performing an approximate full addition on the "image data" as input. The "Image Data" is also taken as input by the approximate subtractor path[17], which approximates the subtraction and outputs the "Difference output" to an 8-bit subtractor. The "Adder Result" and "Subtractor result" are then generated by combining the outputs from the 8-bit RCA and 8-bit Subtractor, respectively[18].



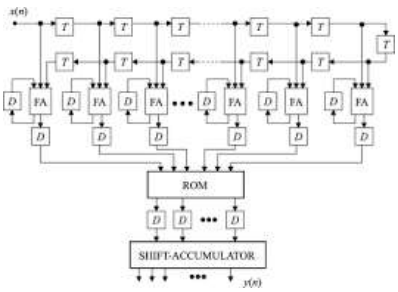
11. Modules Description:

11.1. Fig.3. Approximate Full Adder Module:



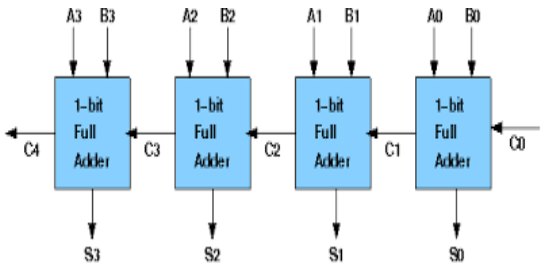
A key component of the suggested system is the Approximate Full Adder Module, which is made to execute addition with less complexity and power usage than conventional full adders. This module probably uses fewer transistors—possibly as few as eight, as indicated in the abstract—and simpler logic. Its purpose is to add controlled approximations to the process, allowing for speed and power efficiency gains at the expense of accuracy[19]. To maximize its performance characteristics, the module probably makes use of strategies like Gate Diffusion Input (GDI) and Dynamic Threshold (DT) implemented with Carbon Nanotube Field Effect Transistors (CNTFETs). This module is essential to the overall operation of the suggested multiplier-free Discrete Cosine Transform (DCT) system since it is a fundamental part of the approximate arithmetic logic unit.

11.2. Fig.4. Approximate Subtractor Module:



An essential part of the suggested system is the Approximate Subtractor Module, which collaborates with the Approximate Full Adder Module to carry out the required arithmetic operations. Even at the expense of a few minor errors, this module is made to perform subtraction with an emphasis on speed and power efficiency. Similar to the adder module, it probably uses a more straightforward design with fewer transistors—possibly as few as eight—and integrates strategies like Gate Diffusion Input (GDI) and Dynamic Threshold (DT) that are implemented with CNTFETs[20]. By making it possible to compute differences efficiently, the approximate subtractor is a key component of the multiplier-free Discrete Cosine Transform (DCT), which is necessary for signal processing operations. This module adds controlled imprecision that stays within acceptable error bounds for the intended applications while improving the system's overall power efficiency.

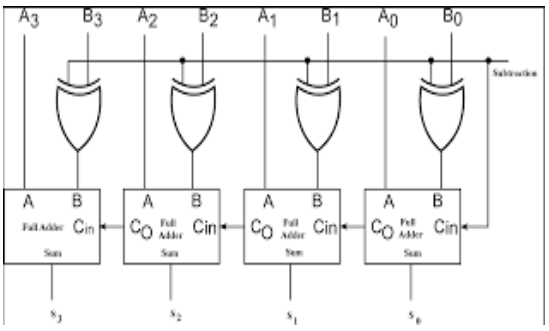
11.3. Fig.5. 8-bit Ripple Carry Adder Module



One of the core arithmetic components of the suggested system is the 8-bit Ripple Carry Adder Module. Eight Approximate Full Adder Modules are used in its construction, with each stage's carry output

linked to the carry input of the subsequent higher-order bit. The adder gets its name from this "ripple" of the carry signal. Although the ripple carry architecture is conceptually straightforward to implement, as the carry signal moves through each stage, a delay may be introduced. However, the use of CNTFET technology and approximate adders in this particular application attempts to partially mitigate this delay. The proposed multiplier-free Discrete Cosine Transform (DCT) system requires the 8-bit Ripple Carry Adder Module in order to perform addition operations on 8-bit data. This architecture is probably selected due to its simplicity and low power consumption, which are in line with the project's overall objectives, even though it may cause carry propagation delay.

11.4. Fig.6. 8-bit Ripple Carry Subtractor Module



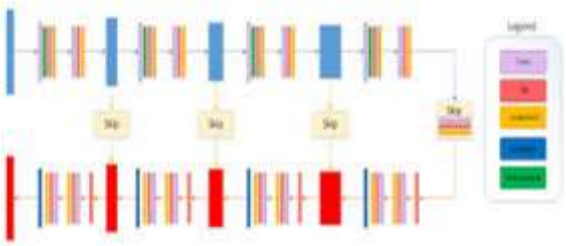
8 bit Approximate Subtractor Modules are cascaded to create the 8-bit Ripple Carry Subtractor Module, a crucial part of the arithmetic unit in the suggested system. This architecture allows subtraction operations on 8-bit data by propagating the borrow signal from each stage to the subsequent higher-order bit, much like the ripple carry adder. Although this design is simple to implement, the borrow signal's ripple may cause a delay that affects the subtraction's overall speed. However, this delay is probably somewhat mitigated by the use of CNTFET technology in conjunction with approximate subtractors, which are made for speed and low power. This module facilitates the required subtraction operations, which are essential to the multiplier-free Discrete Cosine Transform (DCT) necessary for signal processing, enhancing system performance in spite of the ripple carry architecture's intrinsic drawbacks.

11.5.Fig.7. Multiplier-Free DCT Module

The main innovation of the suggested system is the Multiplier-Free DCT Module. It does not use conventional multiplication operations in order to implement the 8-point Discrete Cosine Transform (DCT) algorithm. This is accomplished by utilizing the previously mentioned approximate adder and

subtractor modules in conjunction with particular algorithmic transformations or approximations that enable the DCT to be calculated primarily using addition and subtraction. This module is essential for drastically lowering the DCT's power consumption and computational complexity, which will improve its suitability for resource-constrained applications such as medical implants and portable electronics. However, the objective is to achieve significant performance and energy efficiency gains while maintaining acceptable signal quality for the target applications of image compression and noise reduction.

11.6. Fig.8. Noise Reduction Module (Implicit)



Although the abstract doesn't specify the precise noise reduction techniques used, it's probable that this module makes use of the Discrete Cosine Transform's (DCT) characteristics to reduce noise. Noise, which is frequently high-frequency, can be reduced by adjusting or eliminating the higher frequency DCT coefficients because the DCT concentrates signal energy into lower frequency coefficients. Simple thresholding, in which coefficients below a particular magnitude are set to zero, or more complex filtering methods used in the DCT domain may be a part of this module. It's crucial to remember that the accuracy of the approximate DCT and the noise reduction process are linked; errors introduced by the approximate arithmetic units may have an impact on the noise reduction process.

12.Results:

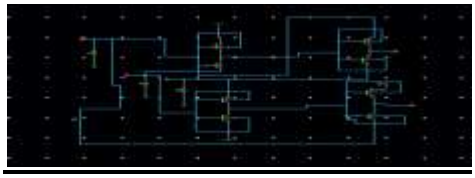


Fig.9 : Schematic Diagram for full Adder

The intricate logic needed for multiplication operations, which involves AND gates, half adders, and possibly full adders—typically constructed using combinations of NAND and NOR gates made by CMOS transistors—is hinted at by the interconnected structure. Whether it's a particular step in the multiplication process or a component of the final adder stage, the precise function being implemented would depend on the particular configuration and connections. A specific feature size and fabrication method are indicated by the use of 180nm technology, which affects the circuit's speed and power consumption. A common layout environment for integrated circuit design is a black background with a grid

pattern, which helps with component placement and connection accuracy.

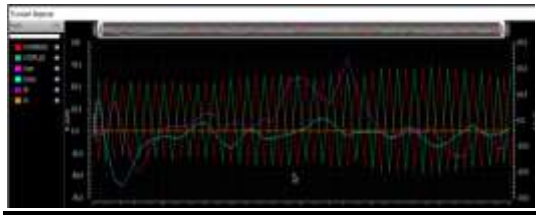


Fig.10.: Output Waveform for Full Adder Transient

The image shows a transient response graph that shows the voltage variations of various circuit nodes over time. It was probably created from a circuit simulation. The label "Transient Response" at the top denotes that a time-domain simulation was used for the analysis, which captured the dynamic behavior of the circuit. Although it isn't labeled specifically, the graph displays several waveforms plotted against time, with time presumably on the x-axis and voltage (V) on the y-axis. According to the labels in the legend on the left, each waveform depicts the voltage at a particular node in the circuit.

Fig.11.:Output Waveform for Full Adder DC Response

"/VO/MINUS", "/VO/PLUS", "/sum", "/carry", "/A", and "/B" are some examples of labels on the left that indicate the precise locations in the circuit where the voltage or current is being measured. These names imply a circuit with inputs "A" and "B" and differential outputs ("/VO/MINUS", "/VO/PLUS"), which may be associated with arithmetic or summing operations ("/sum", "/carry").

Fig.13. Output for loaded image

It acts as a label or description to make it clear that the data, visual representation, or other output that comes from that loaded image is what comes next. This phrase is frequently seen in image editing software, image viewers, web interfaces, and programming environments. It basically serves as a straightforward and easy way to indicate that the information that follows is related to an image that has been loaded.

Fig.12.: Output for Grayscale image

This indicates that an image that has been successfully loaded is directly related to the output. This indicates that an image file has been prepared for viewing, editing,

analysis, or another action by the system or program. This makes it clear that the output is specifically related to a grayscale image manipulation. A grayscale image lacks color information and only has grayscale hues, from black to white.

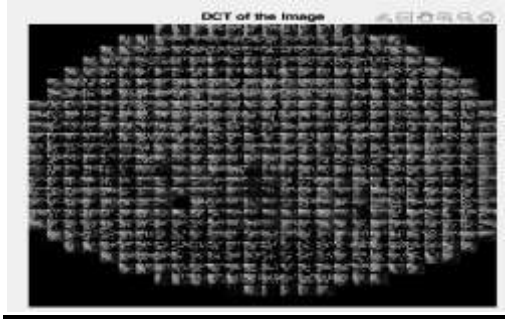


Fig. 14.: Output for Grayscale image

In essence, the Discrete Cosine Transform (DCT) breaks down an image into its individual frequencies. It represents the image as the sum of variously sized cosine waves. This is beneficial since it focuses the majority of the image's energy into a small number of frequency-domain coefficients.

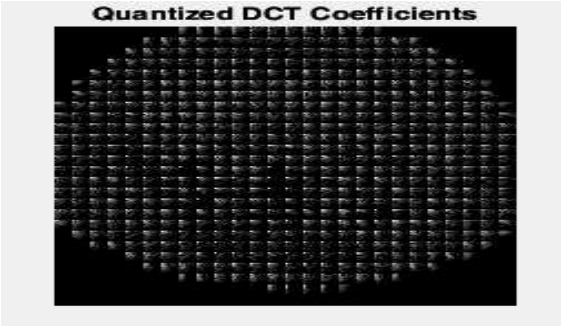


Fig.15.: Output for Quantized DCT Coefficient

In order to lower the quantity of data required to represent the image, the DCT coefficients are adjusted in this critical step. It entails rounding the results to integers after dividing the coefficients by a quantization matrix. In order to achieve compression, this process removes some of the high-frequency information that is less significant and has little effect on the perceived image quality. Although quantization is lossy—some information is lost—it is necessary for effective compression.

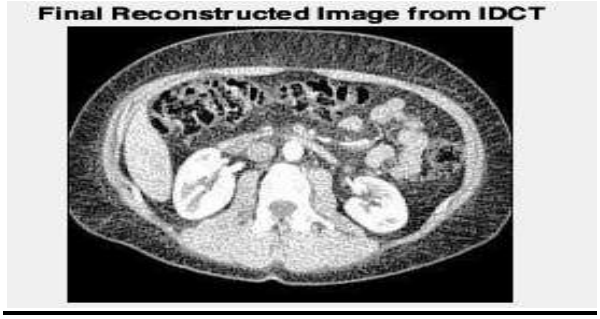


Fig.16.: Output for Reconstruct original image

This suggests an attempt to recreate or come close to the original, unaltered image. This implies that the image has undergone some sort of processing alteration, such as blurring, noise addition, compression, or other methods. The goal of the reconstruction procedure is to undo these changes and retrieve the original image data.

13. Conclusion:

The challenges of creating GaN-based Op-Amps, which are crucial components of analog electronic circuits, are addressed in this research paper. The suggested circuit is specifically implemented in a GaN-IC process, which limits the designer's

options because of the technology's early stages of development. For on-chip high-speed and high-bandwidth feedback circuits, a novel three-stage Op-Amp design is suggested. This design achieves a sufficient DC gain (60 dB) by resistively loading a cascade of differential stages. In order to guarantee closed-loop stability, the paper also presents a novel dual single-Miller frequency compensation method with double pole-zero cancellation. This method is also supported by detailed design equations.

With a high slew rate of over 70 V/µs and a settling time of about 120 ns at room temperature with a gain-bandwidth product of 25 MHz, the designed Op-Amp performs exceptionally well, demonstrating its ability to handle rapid signal changes. Future research will concentrate on creating an output stage to improve current drive capability and a four-stage gain amplifier for increased DC gain.

14. Future enhancement:

To increase device longevity and dependability, ongoing research and development efforts are concentrated on raising the caliber of GaN materials and minimizing flaws. Smaller and more effective power systems are made possible by achieving even higher power densities through the optimization of device design and fabrication processes. It is anticipated that the cost of GaN devices will drop as production scales and technology advance, opening up a greater range of applications. By combining GaN devices with other technologies, like silicon, hybrid solutions that combine the best features of both technologies can be produced. This may result in power electronics systems that are more sophisticated and adaptable. Vertical GaN devices are one example of an innovative device architecture that can further enhance performance and open up new applications.

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