21T Ternary Full Adder Using Carbon Nanotube FETs and Capacitive Threshold Logic

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ABSTRACT:

The design and implementation of a 21-transistor (21T) ternary full adder using carbon nanotube field-effect transistors (CNTFETs) and capacitive threshold logic (CTL) are presented in this paper. By extending traditional binary logic to three states (0, 1, and 2), the ternary logic system provides benefits in terms of increased information density and energy efficiency. The design achieves low power consumption and compactness by utilizing CTL, which uses capacitive components to define logic thresholds. This makes it appropriate for advanced nano electronics. The performance of the ternary full adder is further improved by the use of CNTFETs, which are recognized for having better electrical characteristics than conventional silicon transistors. This results in an increase in speed and power efficiency at smaller technology nodes. Cadence's CINFET tool, a specialized environment for modeling CNTFET-based circuits, is used to simulate the entire adder circuit. The outcomes of the simulation show how effective the 21T design is, emphasizing gains in area, power, and delay. By demonstrating that Capacitive Threshold Logic can be a viable strategy for low-power, high-performance arithmetic operations in future computing systems, this work advances ternary logic systems within the framework of CNTFET technology. The suggested design establishes the foundation for future research into CNTFET-based ternary logic in intricate digital systems in addition to acting as a proof of concept for ternary logic circuits.

Keywords: — 18-nm CINFET ,Look-Up Tables (LUTs), RTL (Register-Transfer Level) design, and synthesis

1. INTRODUCTION:

Capacitive Threshold Logic (CTL) is a promising method for putting ternary logic circuits into practice. By comparing the voltages across capacitive elements to a predetermined threshold, CTL carries out logic operations. Because capacitive components naturally use less energy than conventional switching transistors, this technique has been acknowledged for its potential to lower power consumption. Ternary logic gates can be efficiently and compactly designed using CTL, which makes them perfect for use in high-performance, low-power digital circuits. However, there are a lot of opportunities for future circuit design in the relatively unexplored field of integrating CTL with cutting-edge transistor technologies, like Carbon Nanotube Field-Effect Transistors (CNTFETs). We present a 21-transistor (21T) ternary full adder design in this work that combines the advantages of CNTFETs and Capacitive Threshold Logic.

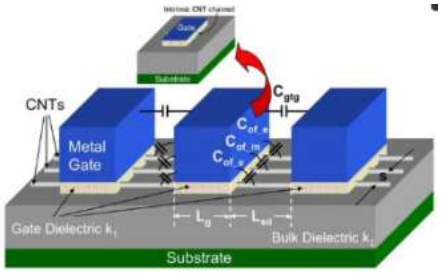

Fig.1. CNFET model

For many digital systems, the ternary full adder is an essential component that carries out the fundamental arithmetic operation of addition[1]. We model the behavior of the complete adder circuit and assess its performance in terms of area, delay, and power consumption using Cadence's CINFET tool. The findings highlight the benefits of ternary logic in conjunction with CNTFET technology and show that the suggested design provides notable improvements over conventional binary logic adders. In addition to demonstrating a working ternary adder, this work investigates the possibilities of ternary circuits based on CNTFETs for the development of high-performance, low-power computing in the future[2].

2.PROJECT OBJECTIVE :

This project's main goal is to use carbon nanotube field-effect transistors (CNTFETs) and capacitive threshold logic (CTL) to design and implement a 21-transistor (21T) ternary full adder[3]. With the goal of offering greater computational efficiency and reduced power consumption in comparison to traditional binary logic circuits, this ternary full adder will show that ternary logic can be used in digital circuits. The design intends to take advantage of CNTFETs' superior electrical characteristics, such as their high electron mobility and low power dissipation, in order to make the adder appropriate for upcoming low-power, high-performance digital systems[4].

$$P = P_s + P_d$$

$$Static: P_s = P_{leakage} * k1 * N * V_{dd}^2 / R$$

$$Dynamic: P_d = k2 * \sum C_l * V_{dd}^2 * f$$

where:

- N: Transistors count in the circuit,
- V_{dd}: Power Supply,
- k_1: Ratio of diode-connected transistors,
- R: Diode-connected transistor resistivity,
- k_2: Ratio of switching capacitors,
- C_l: Load Capacitor or Internal Capacitor,
- f: Clock frequency of the circuit.

3. PROBLEM STATEMENT:

Furthermore, there are both opportunities and challenges in circuit design and simulation when it comes to integrating cutting-edge technologies like Carbon Nanotube Field-Effect Transistors (CNTFETs) into ternary logic circuits. A high-performance, low-power ternary full adder that makes use of CNTFETs and Capacitive Threshold Logic (CTL) is the issue this project attempts to solve. A CNTFET is a type of FET in which the channel between the source and drain is made up of one or more CNTs. CNTs fall into two categories: single walled CNTs (SWCNTs), which have a single graphite cylinder, and multi-walled CNTs, which have several concentric graphite cylinders. The graphite sheet is wrapped in the direction of the chiral vector in order to construct SWCNT.

Due to the limitations of silicon transistors and conventional binary logic, existing digital circuits are having difficulty scaling in terms of both performance and power efficiency[5]. By creating a ternary full adder that takes advantage of the superior electrical properties of CNTFETs and maximizes the benefits of ternary logic, this project aims to close the gap and eventually make it possible to design faster and more energy-efficient digital circuits.

4. PROJECT SCOPE : The design and simulation of a 21T ternary full adder utilizing carbon nanotube field-effect transistors (CNTFETs) and capacitive threshold logic (CTL) are the main objectives of this project. From the basic logic gates based on ternary voltage states to the finished adder structure, the scope encompasses the development of the ternary full adder circuit[6]. CNTFETs will be used in the design process to construct the logic gates, taking advantage of their low power dissipation and speed. Cadence's CINFET tool will be used for simulation, enabling precise assessment of the circuit's performance parameters, such as power, delay, and area. Additionally, a thorough evaluation of the ternary full adder's performance in comparison to conventional binary adders will be part of the project.

The comparison will concentrate on aspects like overall design viability for future nanoelectronics, energy consumption, and computational efficiency. In addition to showing how ternary logic circuits can be used practically, the scope will investigate how CNTFETs might be used to build more scalable and effective circuits for upcoming computer applications.

5. METHODOLOGY:

This project employs the Ternary Full Adder Algorithm, which is implemented with CNTFET-based logic gates in conjunction with Capacitive Threshold Logic (CTL). The algorithm's specific steps include building ternary logic gates (like ternary AND, OR, and XOR gates) and then building a ternary full adder that calculates the sum and carry-out from three ternary input values.

The Cadence CINFET tool is used to simulate the behavior of the entire adder in order to verify power and delay metrics, and the logic gates' performance is optimized based on the capacitive elements' voltage threshold conditions[7].

6. EXISTING SYSTEM :

The majority of contemporary digital circuits are built on top of conventional binary logic systems, which employ two states (0 and 1). Binary adders, like the conventional full adder, which usually employ CMOS (Complementary Metal-Oxide-Semiconductor) technology, are the foundation of these systems. Despite being widely used because of its ease of use and proven fabrication methods, binary logic has drawbacks in high-density and low-power applications, particularly as technology nodes get smaller.

Furthermore, binary adders are less effective for some sophisticated applications[8], such as those in low-power, high-performance computing systems, due to their reliance on numerous logic gates and high power and area consumption.

7. PROPOSED SYSTEM:

The suggested system makes use of a 21-transistor (21T) ternary full adder design that integrates Carbon Nanotube Field-Effect Transistors (CNTFETs) and Capacitive Threshold Logic (CTL). A more effective method of representing information is provided by ternary logic, which employs three different states (0, 1, and 2), increasing information density and improving silicon area utilization[9]. Compared to conventional binary logic circuits, CTL uses capacitive components to define logic thresholds, resulting in smaller designs and lower power consumption.

Fig. 1. Circuit diagram of 21T CINFET

Because CNTFETs have better electrical characteristics than silicon transistors, like higher carrier mobility and a better subthreshold slope, they improve the adder design's speed and power efficiency, which makes them ideal for advanced nanoelectronics.

8. SURVEY OF LITERATURE:

Shivendra Kumar, Bhavana Sharma P. Srivastava clarifies For bit interleaving applications, a low power single ended 13T CINFET cell has been proposed in this process. To create a stable CINFET cell with superior performance over the current designs, a column-aware scheme is employed in the cell. Better read performance and robust read operation are demonstrated by the suggested CINFET cell, which also uses less power. The power consumption, delay, and power delay product (PDP) of this proposed 13T CINFET have been compared to those of the conventional 6TCINFET and the current 9T CINFET (with bit-interleaving capability) at 1.8V, 1.6V, and 1.4V supply voltages, among others.[10] The suggested design's superiority over the current designs is confirmed by analyzing the simulation results, which are performed on Cadence Virtuoso at 180nm CMOS technology. In terms of power and PDP, the suggested 13T CINFET performs better across the board. The suggested circuit saves 72.46% of the power at 1.8V when compared to a standard 6T CINFET cell, and notable improvements are also seen at other supply voltages.

In the end, a CNFET's gate width (WGate) is roughly equal to the number of CNTs

beneath the gate terminal[11], N, times the pitch, or distance between the centers of two neighboring CNTs.

$$\overrightarrow{\text{Chiral}} = n_1\vec{a_1} + n_2\vec{a_2}$$

$$D_{CNT} = \frac{\left|\overrightarrow{\text{Chiral}}\right|}{\pi} = \frac{a\sqrt{{n_1}^2 + {n_2}^2 + n_1 \times n_2}}{\pi}$$

$$V_{Th} \simeq \frac{E_g}{2e} = \frac{aV_\pi}{\sqrt{3}eD_{CNT}}$$

$$W_{Gate} = \max\left(W_{\min}, N \times Pitch\right)$$

Addition: A THA is positioned in the least significant position when two numbers are added. The set {0, 1}3 includes a THA's output carry. As a result, either "0" or "1" is sent to the input carry port of the TFA that comes after it in the next position. Therefore, it does not generate '2' for the output carry, and any TFA in a Ripple-Carry Adder (RCA) does not have to be a complete one[12]. Subtraction: Since the sum of a0 and b0 must be raised by one unit in the least significant position, the initial THA in an RCA must be swapped out for a TFA in order to transform an adder into a subtractor. Nevertheless, a partial TFA that can compute a0+b0+1 can still be used to accomplish this.

9. MODULES IMPLEMENTATION:

9.1. CINFET CMOS Design:

In any kind of memory architecture, the CINFET architecture is primarily utilized for single cell storage. Additionally, the architecture uses less power to store 1-bit data. Because of the internal memory placement, the CINFET architecture uses less energy. as well as to create the CINFET cache architecture. The STT-MRAM CACHE memory architecture is applied in the CINFET CMOS design in order to lower overall power consumption and boost performance.

9.2 21T Ternary:

Here, bit-lines BLN and BL have been connected to the output nodes QN and Q, respectively, of two access transistors, pMOS transistors P5 and P6. A word-line WL determines whether they are ON or OFF. Note that when a pMOS transistor is struck by a radiation particle,

When a radiation particle hits a MOS transistor, only a positive transient pulse (0→1 or 1→1 transient pulse) can be produced; conversely, only a negative transient pulse (1→ 0 or 0→0 transient pulse) can be induced.Therefore, pMOS transistors (i.e., transistors P6 and P5) are used as access transistors to prevent a negative transient pulse caused by a radiation particle in the Q and QN nodes.

1) Transistors P1, P4, P7, N2, and N3 are ON and the rest are OFF when word-line WL is high state 1. As a result, nodes Q and QN retain their original data and are not altered.

2) Two bit-lines, BL and BLN, must be recharged to supply voltage VDD prior to the read operation being carried out in the proposed 21T memory cell. When the word-line WL is in the 0 state following a read operation, the output node Q will remain in its initial state of 1. Nevertheless, bit line BLN will be discharged since transistors P5, P7, and N2 are ON. The stored data will then be output by the memory's differential sense amplifier after the voltage difference between two bit-lines, BL and BLN, has been determined.

3) Word-line WL and bit line BL must be in the 0 state and bit line BLN must be in the 1 state in order to write data 0 into the suggested 21T cell. Node Q will then be depressed to 0 state, and node QN will be raised to 1 state.

There will be transistors P1, P4, P7, N2, and N3 OFF and transistors P2, P3, P8, N1, and N4 ON. The stored data will be 0 when word-line WL is brought back to high state 1. This indicates that the

suggested RHBD 21T memory cell can successfully receive data 0.

.9.3. Cell Schematic and Write/Read Timing:

Here, bit-lines BLN and BL have been connected to the output nodes QN and Q, respectively, of two access transistors, pMOS transistors P5 and P6. A word-line WL determines whether they are ON or OFF. It should be mentioned that only a positive transient pulse (0→1 or 1→1 transient pulse) can be produced when a radiation particle strikes a pMOS transistor; conversely, only a negative transient pulse (1→ 0 or 0→0 transient pulse) can be induced when a radiation particle strikes an nMOS transistor. Therefore, pMOS transistors (i.e., transistors P6 and P5) are used as access transistors to prevent a negative transient pulse caused by a radiation particle in the Q and QN nodes.

1)Transistors P1, P4, P7, N2, and N3 are ON and the rest are OFF when word-line WL is high state 1. As a result, nodes Q and QN retain their original data and are not altered.

2) Two bit-lines, BL and BLN, must be recharged to supply voltage VDD prior to the read operation being carried out in the proposed 21T memory cell. When the word-line WL is in the 0 state following a read operation, the output node Q will remain in its initial state of 1. Nevertheless, bit line BLN will be discharged since transistors P5, P7, and N2 are ON. The stored data will then be output by the memory's differential sense amplifier after the voltage difference between two bit-lines, BL and BLN, has been determined.

1) 9.4. SEU Recovery Analysis

Since node Q's stored value is in the 1 state and it is connected to the drain area of OFF pMOS transistors P6 and P8, it is not a sensitive node. Thus, in accordance with the upset physical mechanism, only a positive pulse is induced when node Q is struck; that is, node Q will be impacted by a 1 → 1 transient pulse, ensuring that the stored value of node Q remains unchanged.

1) Transistors P1 and P4 will be off when node QN is perturbed by a radiation particle, which will cause node QN to be pulled up to state 1. Nodes Q and S1 will then maintain their initial logic 1 state without experiencing a drop in voltage.

As a result, node S0 maintains its initial 0 state and transistor N3 won't be turned off. Node QN will be pulled back to its initial state of 0 after transistors P7 and N2 are in the ON state.

2) A radiation particle will alter its value when it hits node S0. Then, node S1 will be pulled down to 0 when transistor P7 is momentarily turned OFF and transistor N1 is momentarily turned ON. However, transistors N4 and P1 maintain their OFF and ON states, respectively, due to the capacitive effect, which prevents node QN from changing to the 1 state. As a result, node S1 can return to its initial 1 state and node Q will remain unchanged through transistor P4.

Ultimately, node S0 will be pulled back to its initial 0 state when transistor N3 is turned on.

3) Transistors N3 and P8 will turn OFF and ON, respectively, when a radiation particle changes the state of node S1 from its initial 1 state to 0. Transistor P1 stays ON since nodes Q, QN, and S0's voltages won't change. Consequently, transistor P1 will be turned on, pulling node S1 back to its initial 1 state[13].

4) Several sensitive nodes may be impacted when a radiation particle hits a semiconductor device due to the charge sharing effect. Transistors P7 and P8 in the suggested 21T memory cell will momentarily turn OFF and ON, respectively, if node pair S0–S1 is disturbed.

The analysis then becomes identical to the analysis when node S0's stored value is altered. As a result, nodes S0 and S1 will be dragged back to their initial states.

5) The voltage of node pairs S0–QN or S1–QN can be altered due to the charge sharing effect, which will alter the proposed 21T cell's stored state. Node Q will be pulled down to state 0 since transistors P8 and N4 will both be ON. A write0 operation is comparable to this situation.

10. RESULTS:

Fig.2. Compilation

Fig.3. Cadence Virtuoso 6.8

Fig.4. Results analysis of 21T process

Area	110 uA
Power	1micro watt to 16 microwatt depends on temperature values
Delay	0.5ms

Fig.5. Calculation of Area, power, delay

10. CONCLUSION :

To sum up, the suggested 21T Ternary cell employing CINFET-based CMOS technology provides notable enhancements over conventional CINFET designs, tackling important issues like performance, stability, and leakage power. Through the use of CINFET transistors and sophisticated power-reduction techniques, the design maintains high-speed operation while achieving significant energy efficiency. The CINFET cell's computational capabilities are further improved by the incorporation of an L1 distance calculation mechanism, which qualifies it for use in data-intensive tasks, IoT systems, and mobile devices. All things considered, the enhanced 21T Ternary cell shows promise as a solution for next-generation memory systems, providing a balance between performance[14], scalability, and power efficiency in progressively more advanced and compact technological nodes.

11.FUTURE ENCHANCEMENT:

Future improvements to the suggested 21T Ternary cell design could involve investigating the incorporation of more sophisticated transistor technologies, like tunnel FETs (TFETs) or negative capacitance FETs (NC-FETs), to further lower power consumption and speed up switching. To further maximize energy efficiency, integrating machine learning algorithms for dynamic power management may also allow adaptive control of the CINFET cell's performance in response to workload demands in real time. The design may be better suited for high-density memory applications if more research is done on multi-level cells or 3D stacking, which could increase memory density and lower area overhead. Error-correcting codes (ECC) and other fault tolerance techniques may also be used to increase reliability in mission-critical applications, offering a strong defense against next-generation memory technologies.

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