Design and Analysis Low Power 8×8SRAM Array using MT-CMOS Technique and VT-CMOS Technique

E. Srinivas[1],
Associate professor,
Anurag group of institution,
(srinivasece@cvsr.ac.in).

T.Annamani[2]
Asst.Professor,
Anurag group ofinstitution,
(annamaniece@cvsr.ac.in)

ABSTRACT: ***Storage of data is required in all the high performance VLSI circuits used today. The need for the day is large amount of data to be stored and accessed as fast as possible, The Static random access memory (SRAM) is widely used memory in consumer electronics. So, it is need to be a ultra-low power design. To obtain low power SRAM cell need to apply low power techniques. Firstly, Design the 8T SRAM cell check it's write and read operation for that 8×8 SRAM array is to be designed, The essential circuits required to design SRAM array are 3 to 8 Decoder, Pre-charge circuit, Write Driver, Sense amplifier after this initiate the implementation of low power techniques to the SRAM cell. Here two low power techniques are used for designing of SRAM Cell. The Low power techniques are Multi Threshold CMOS (MTCMOS),Variable ThresholdCMOS(VTCMOS).The simulation results and graphical plots demonstrate the most suitable low power technique to reduce the dynamic power consumption of 8T SRAM cell. For Designing of low power 8X8 SRAM Array using 180 nm CMOS technology.***

KEYWORDS: Low power, Static random access memory, SRAM Array, Multi Threshold CMOSTechnique (MTCMOS), Variable Threshold CMOSTechnique (VTCMOS).

1 .INTRODUCTION

With advancing technology, there is always an increase in demand for larger data storage capacity. This has driven the fabrication technology and memory development towards more compact design rules and towards higher data storage densities. A variety of memories are available to store and access the information stored. According to ones need one may select a read only memory which is generally used in microcontrollers or a read write memory that is generally used in microprocessors. In comparison to DRAM though SRAM requires more space, it is easily fabricated and is much faster. Dynamic RAM unlike the Static RAM needs to be refreshed after equal intervals of time. Hence for SRAMs the standby power is very low despite of high density of transistors. SRAM cells have high noise immune due to larger noise margins, and have ability. The most important application of SRAM is in CPU cache memories, small on-chip memories, FIFOs or other buffers. Here, design of 8x8 SRAM array chip and analyse the area and delay of the entire chip.

1.1 Design of 8T SRAM Cell

The SRAM cell that we considered in this paper is "**8T SRAM Cell**" which consists of two crossly coupled inverters and access transistors to read and write the data and additional two symmetrical NMOS transistors (N5 and N6) placed opposite to the access transistor. Instead of 6T SRAM Cell the 8T SRAM Cell is used. Because this cell has low leakage power compared to the conventional 6T SRAM Cell. But the addition of those two NMOS transistors (N5 and N6) the power consumption of this cell increased.

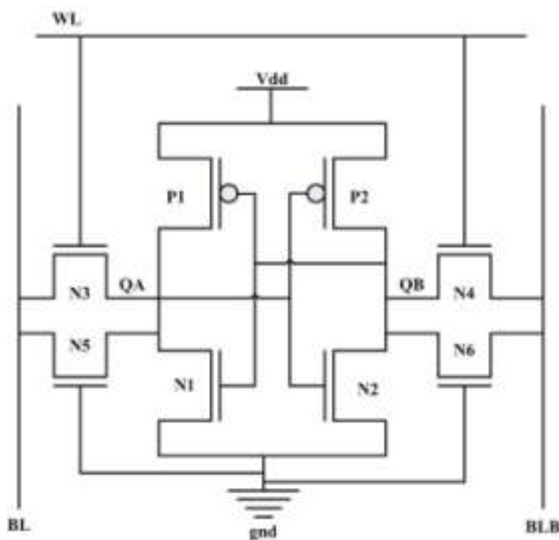

Fig 1: block diagram of 8T SRAM Cell.

The supply voltage of this cell is 800.0mv. For write operation drive the input value and its compliment to the bitline (BL) and bitline_bar (BLB) then raise the wordline (WL). Pre charging of bitline (BL) and bitline_bar(BLB) is set to high and let them float. The Q_A and Q_B are the outputs of these two cross coupled inverters.

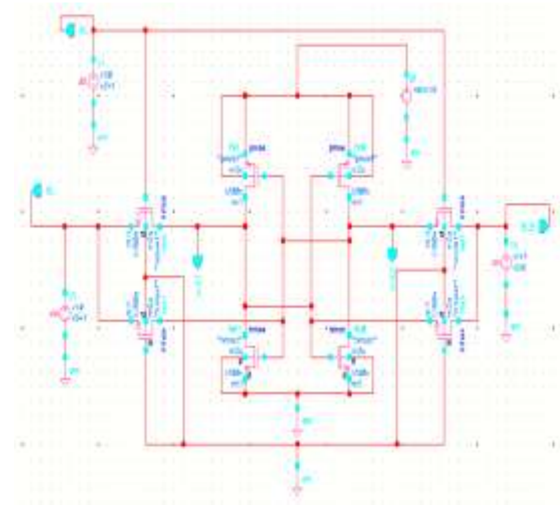

Fig 2: Schematic of 8T SRAM Cell

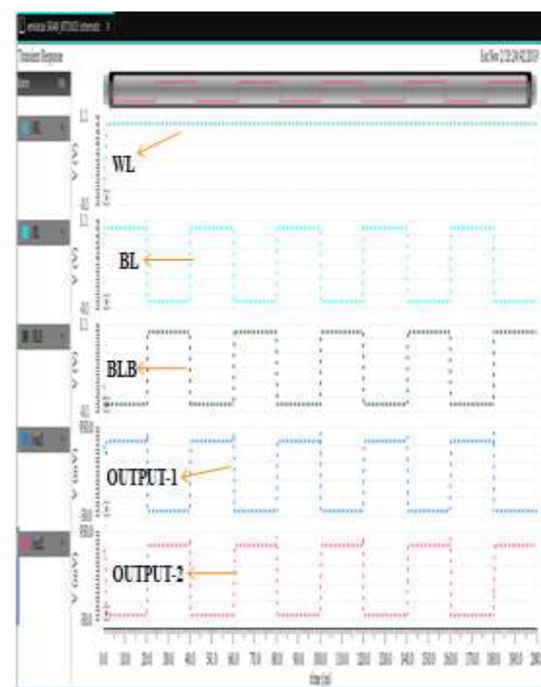

Fig 3: Transient response of 8T SRAM Cell

By observing the transient response of 8T SRAM cell it indicates working nature of the cross coupled inverters the word line is maintained at 1V constantly, Q_A is compliment to bitline (BL) and Q_B is compliment to bitline_bar (BLB) as shown in the Fig 3.

1.2. Block diagram of Generic SRAM Array

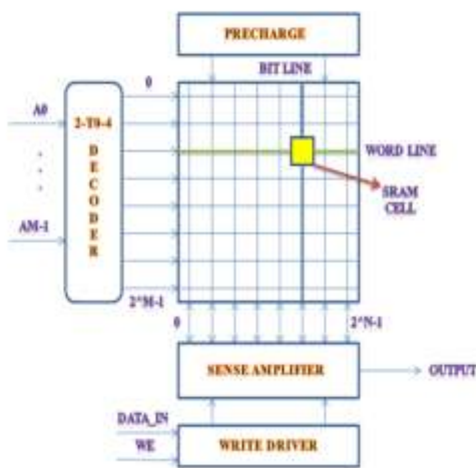

Fig 4: block diagram generic SRAM Array

To Design SRAM Array, Firstlydesign sub circuits of SRAM Array are essential circuits and plays crucial role in designing of SRAM Array. They are 3 to 8 Decoder,Pre-charge circuit, Write Driver, Sense amplifier, SRAM cell.

1.3. Design of 3 to 8 Decoder

The decoder is a logic circuit that accepts the set of inputs that represent a binary number and activates that output which corresponding to the input binary number. A decoder has 'n' inputs and 2^n output lines.

The 3-to-8 decoder operates according to the Truth table as shown in Table 1.

- The 3-bit input is A_0, A_1,$A_2$and the Eight outputs are D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7.
- If the input is the binary number i, and then output Di is uniquely true.
- For example, if the input A_0, A_1, A_2=01, then output D_0 is true, and D_1, D_2, D_3, D_4, D_5, D_6, D_7 are all false.
- This circuit "decodes" a binary number into a "one-of-eight" code.

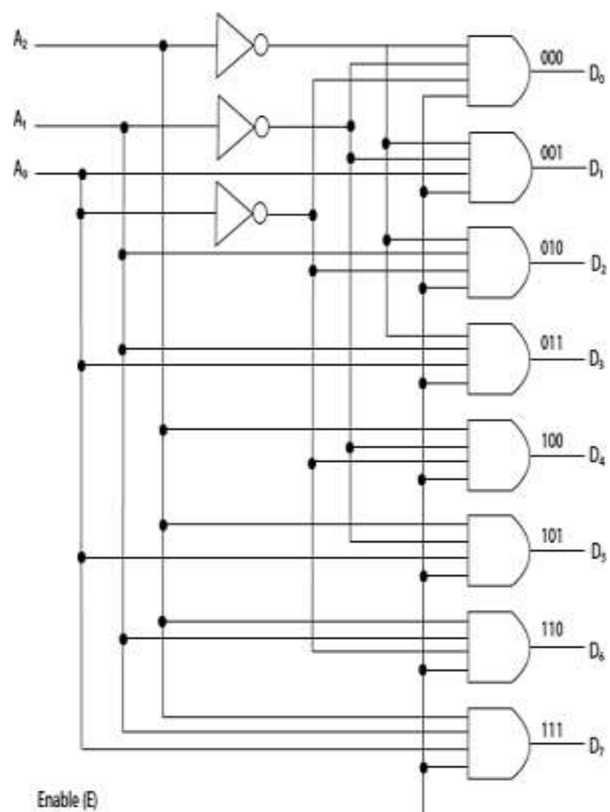

Fig 5: block diagram of 3 to 8 Decoder

A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Table 1. Truth Table of 3 to 8 Decoder

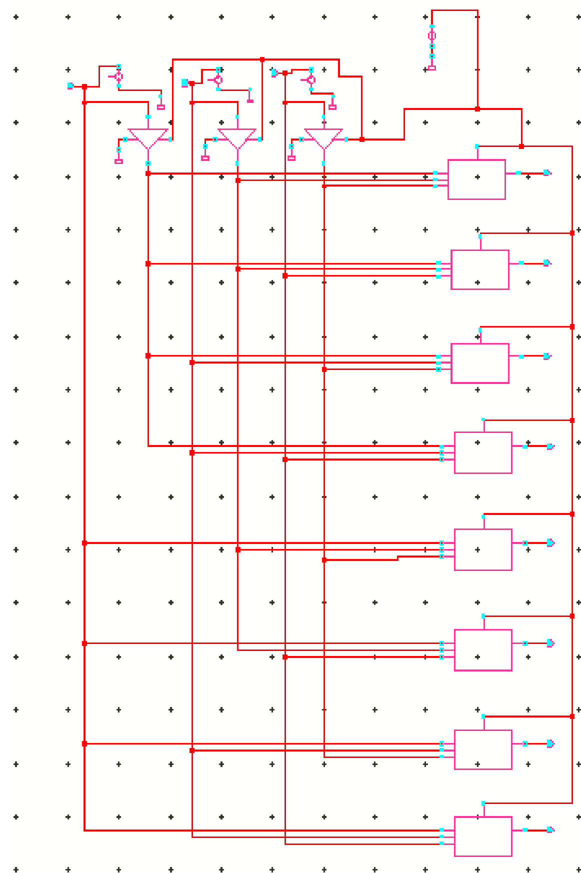

Fig 6: Schematic of 3 to 8 Decoder

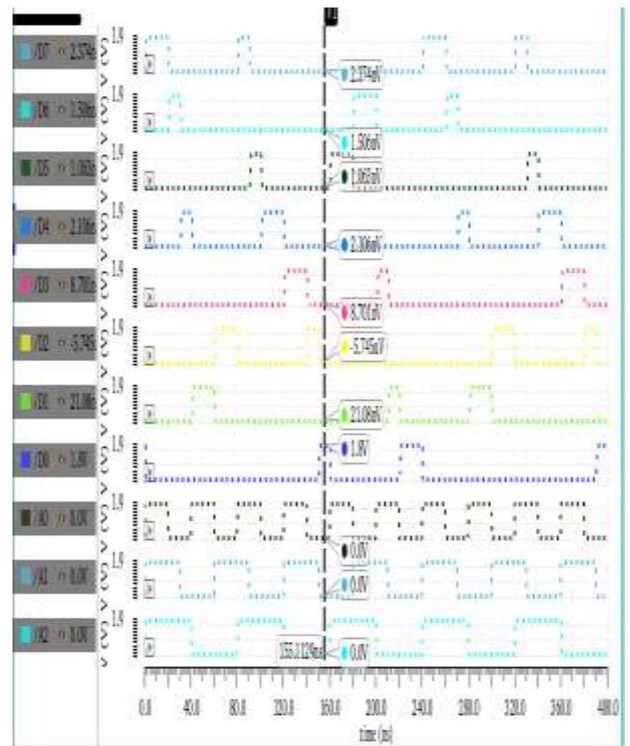

Fig 7: Transient response of 3 to8 Decoder

1.4 Design Ff Pre-Charge Circuit

The pre-charge circuit is one of the vital componentthat is persistently employed within SRAM cell. The work of the pre-charge is to charge the bit and bitline-bar to the power supply V_{dd}=1.8v. The pre-charge circuits authorize the bit lines to be charged high at all times aside from throughout read and write operation. The width needed for PMOS is at least i.e. 240 nm and length is fixed to 180 nm. For

every segment single pre-charge circuit is utilized.

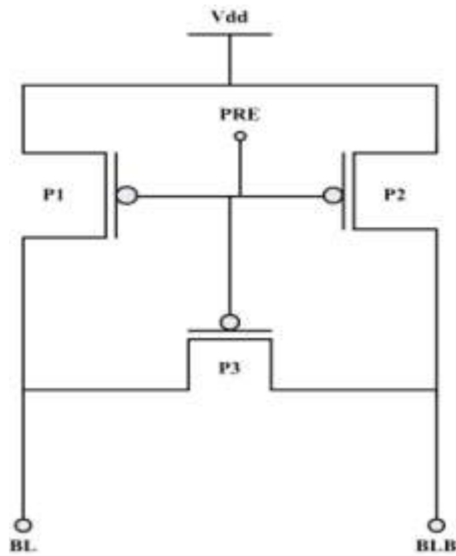

Fig 8: block diagram of Pre-charge circuit

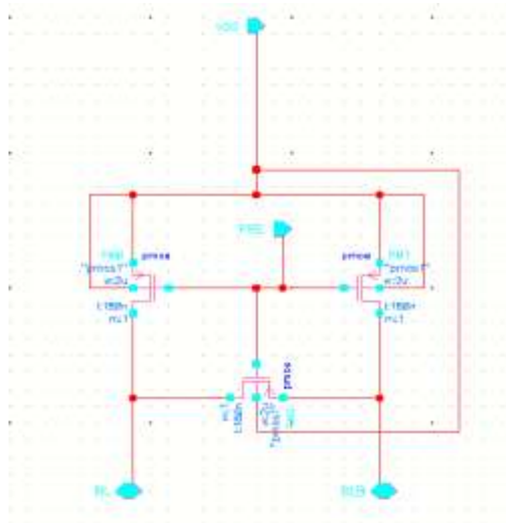

Fig 9: Schematic of Pre-charge circuit

Pre-charge of the power line voltages in a high voltage DC application is a preliminary mode which limits the inrush current during the power up procedure.

The pre-charge that holds bit lines at positive voltage makes it possible to amplify that differential signals to a useful logic level.

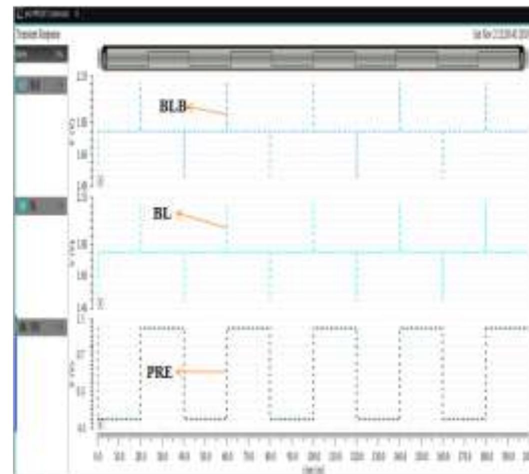

Fig 10: Transient response of Pre-charge circuit

1.5 Design of Write Driver Circuit

The write driver circuit is one of the vital componentin the SRAM array design. The job of the write driver is to keep thebit line and bitline-bar to ground potential for the further next level of its work.

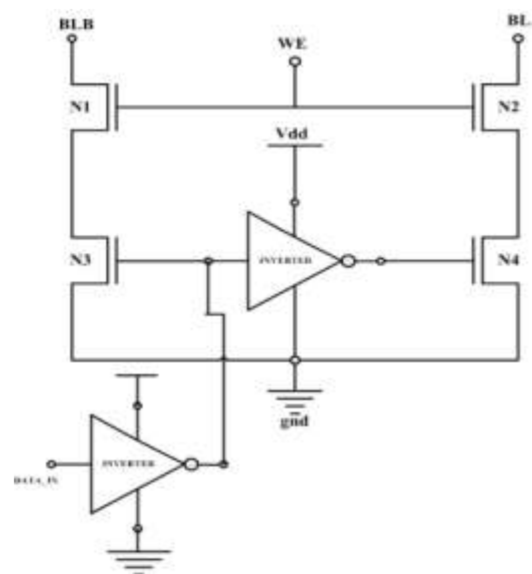

Fig 11: block diagram of Write driver

Before this the bit line and bitline-bar are being charged maximum supply voltage of V_{dd}. By the usage pre-charge circuit it will get charged and after that it gets discharged.

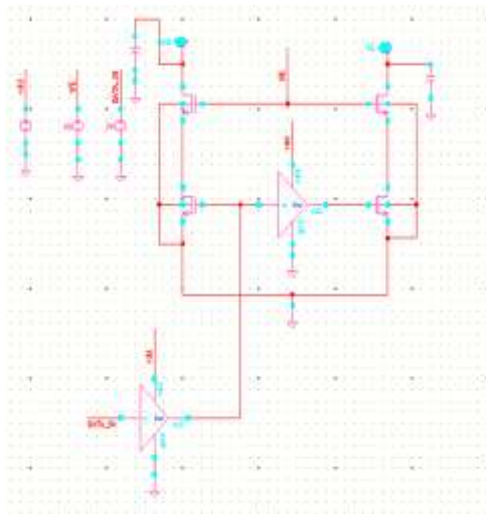

Fig 12: Schematic of Write driver

The two logics are given to the two points of the junction of the NMOS. i.e0 and 1.The bit line which is nearer to the 0 logic it gets discharged first after that its logic gets inverted. In this way the bit line and bitline-bar gets discharged to the ground. With this kind of operation the bit line and bit line bar gets discharged. So that the voltage difference between bit line and ground, bit line bar and ground is zero. So that another data can be easily retrieved by the memory cell.

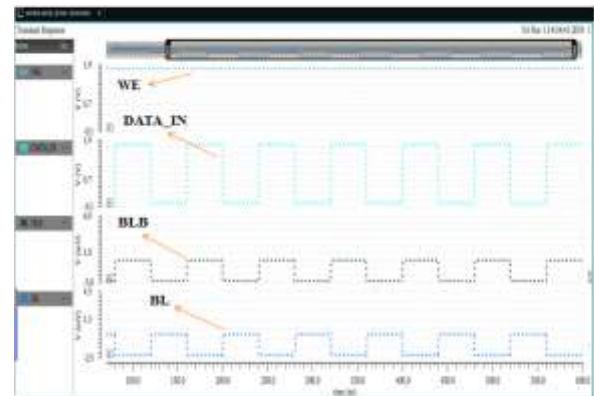

Fig 13: Transient response of Write Driver

1.6Design of Sense Amplifier

The Sense amplifiers are the essential component in the SRAM memory design. The job of sense amplifier is to sense the bit line and bitline-bar for proper observing action. It improves the read and write speed of the SRAM memory cell. Another job is to achieve the low power consumption operation in memory design.

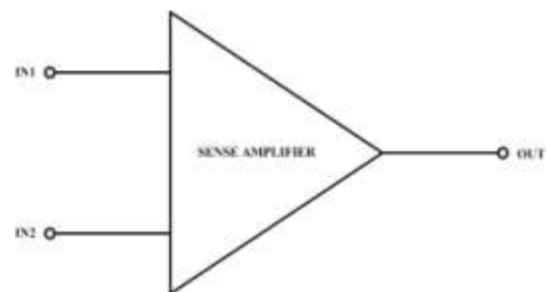

Fig 14: block diagram of Sense Amplifier

The sense amplifiers primary utilized to amplification of the voltage difference is being produced on the bit line and bitline-bar at the time of operation.As we know that in SRAM operation we didn't do refresh of the memory for the further process, as the each segment has one sense amplifier for the single output.So, it can get properuse of the sense amplifier in the designing circuit. These is the various parameters of a sense amplifier are

Gain A =Vout/Vin

Sensitivity S is Vin min-least noticeable signal.

Rise time t-rise, fall time t-fall -10% to 90%.

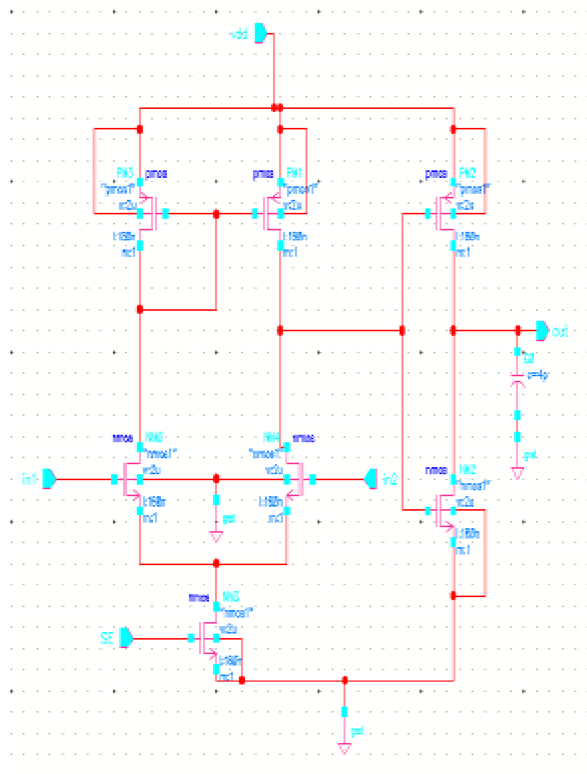

Fig 15: Schematic of Sense Amplifier

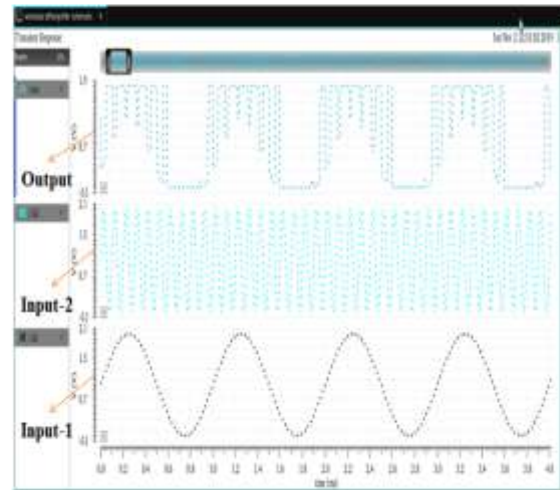

Fig 16: Transient response of sense amplifier

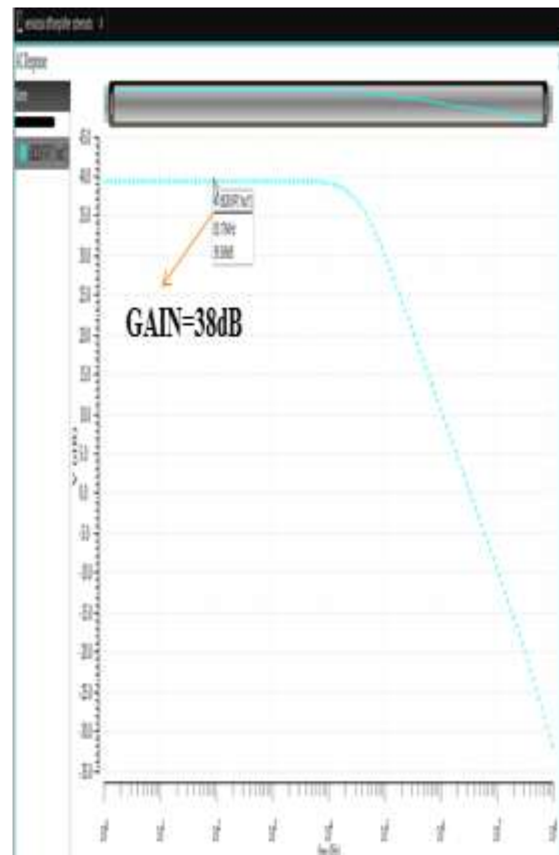

Fig 17: Gain of sense amplifier

1.7 Designof 8×8 SRAM Array

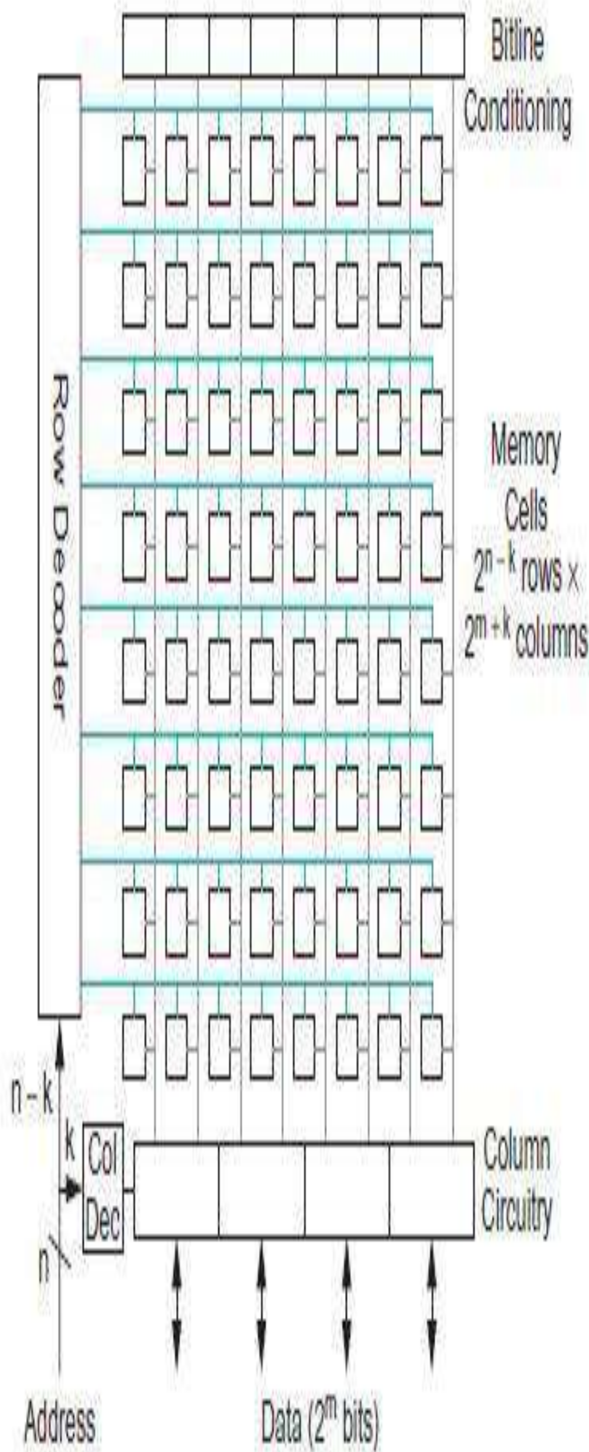

Fig 18: Block diagram of 8×8 SRAM Array

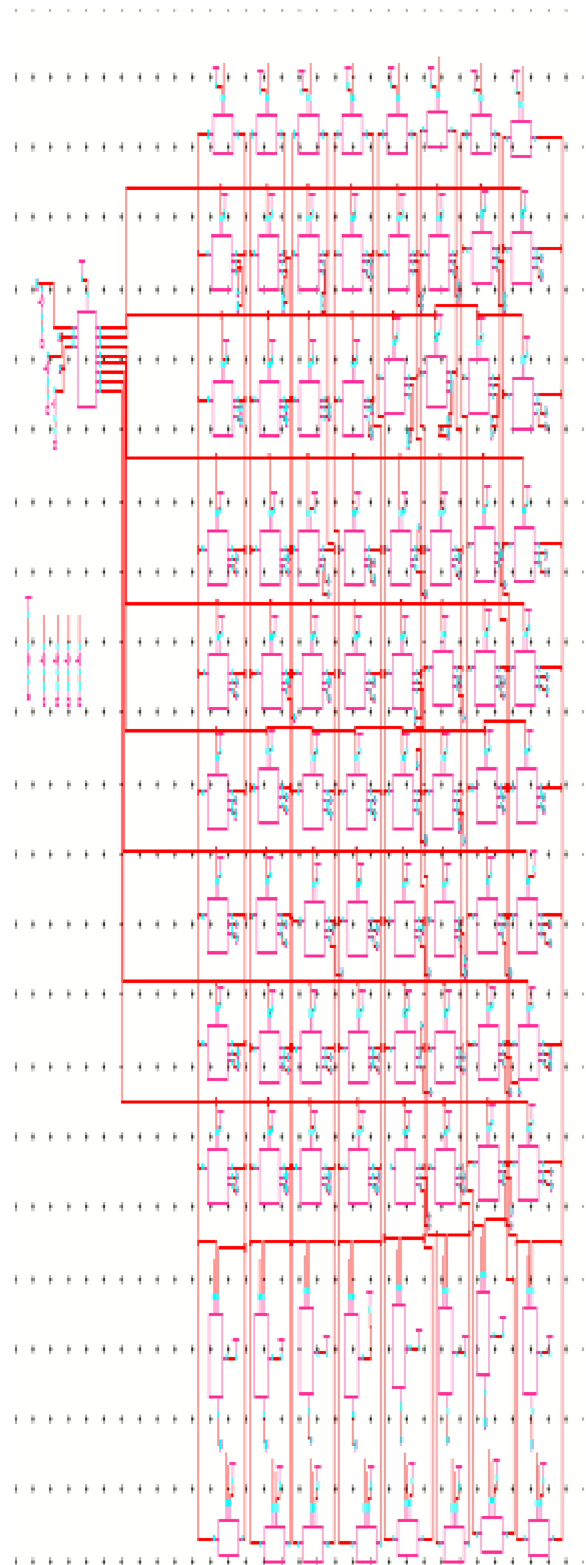

Fig 19: Schematic of 8×8 SRAM Array

Write Operation

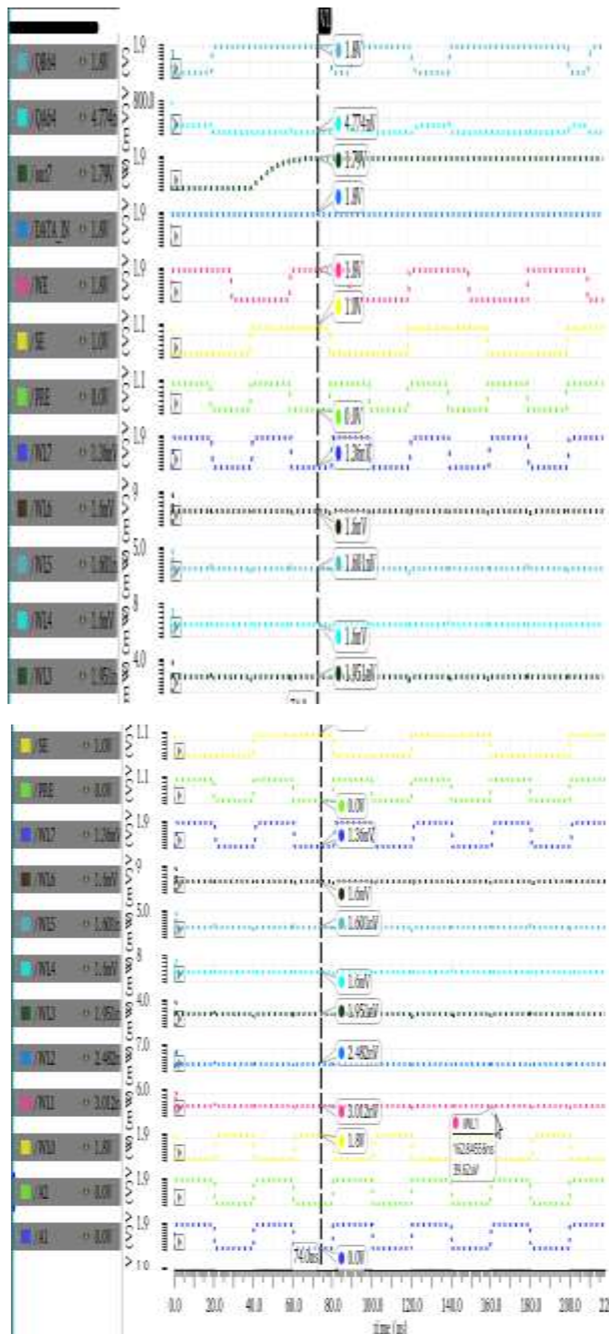

Fig 20: Transient response Write 0 and Write 1 operation

The Transient response for the write 0 and write 1 operation is shown in Fig. 20. In the read operation, also here the WL_7 and WL_0 are activated in order to perform the required operations. The WL_7 when it is high at a point the WL_0 is low, resulting in write 1 operation at Q_{A0} and write 0 operation at Q_{B0}. Therefore, the write 0 and write 1 operations are verified.

Read Operation:

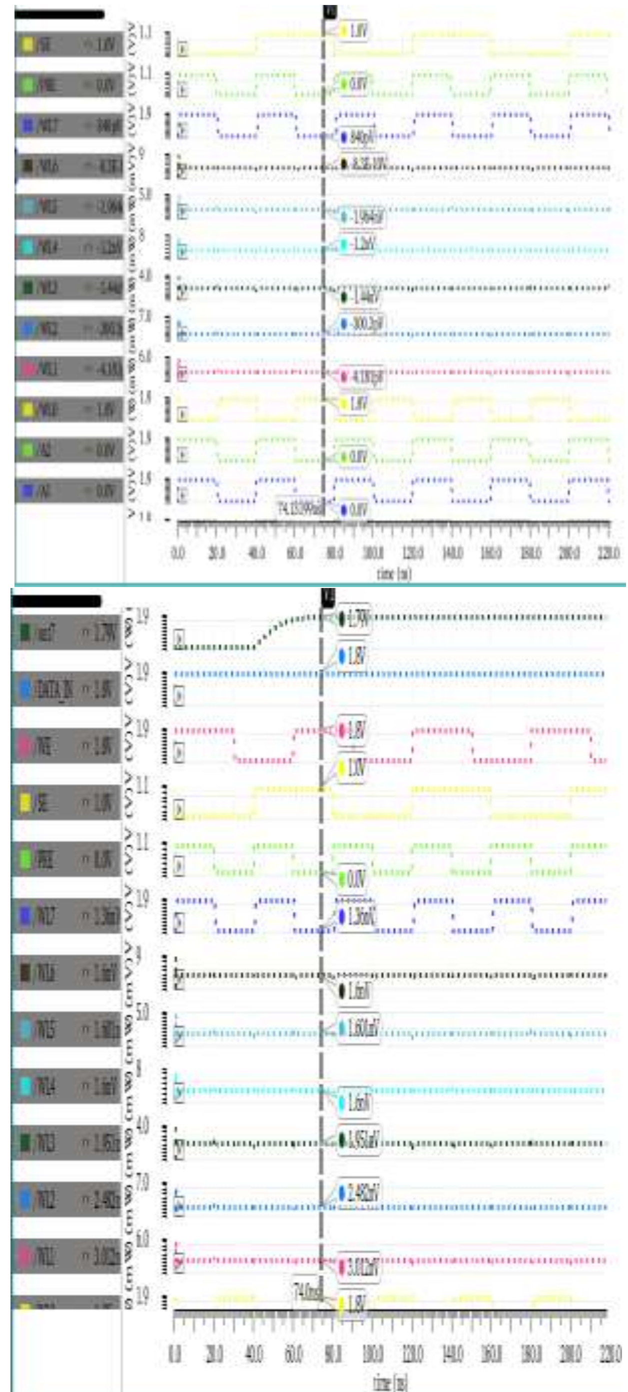

Fig 21: Transient response for Read operation

The transient response as shown in the above results, in read operation when both the inputs get low at that time data is being kept at the constant value. When WL_7goes from high to low and WL_0 goes from low to high with sense enable gets on it get confirmed for the read

Operation of the memory cell.

2. LOW POWER TECHNIQUES

2.1 MULTI THRESHOLD CMOS TECHNIQUE(MTCMOS)

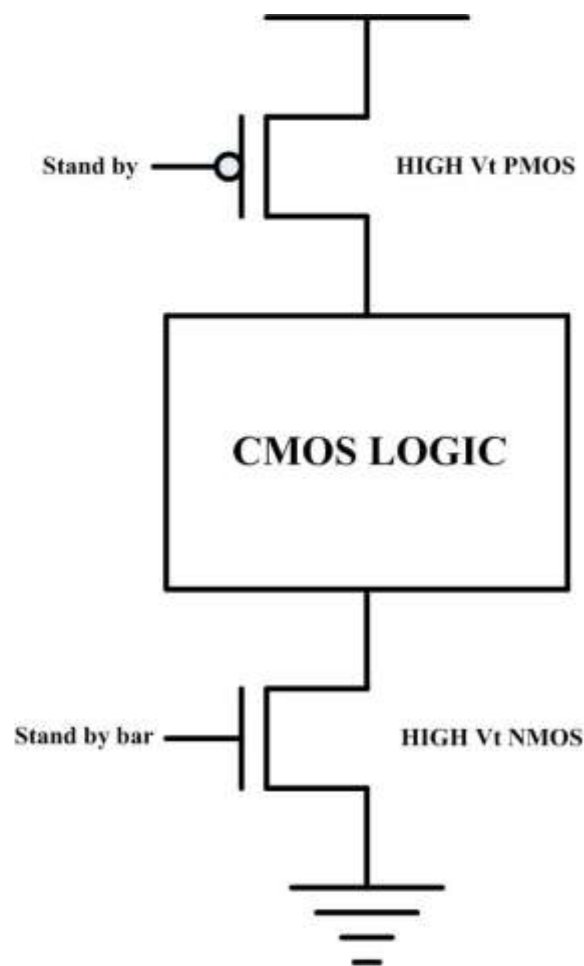

Fig.22: Block diagram of MT-CMOS Technique

This MT-CMOS Technique has high speed operation with low power consumption. It uses the power gating process. It prevents sub threshold leakage in standby mode. Power gating is a technique used in IC design to reduce power consumption by shutting off the current to blocks of the circuit that are not in use.

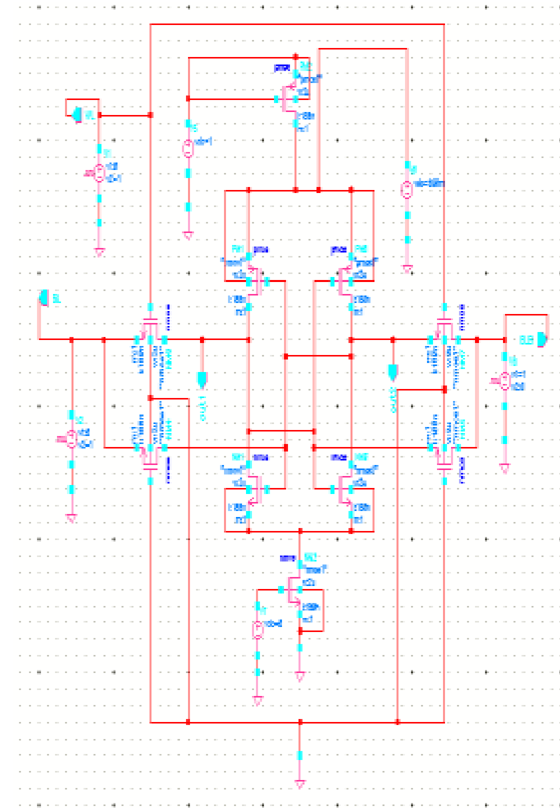

Fig 23: Schematic of MT-CMOS 8T SRAM cell

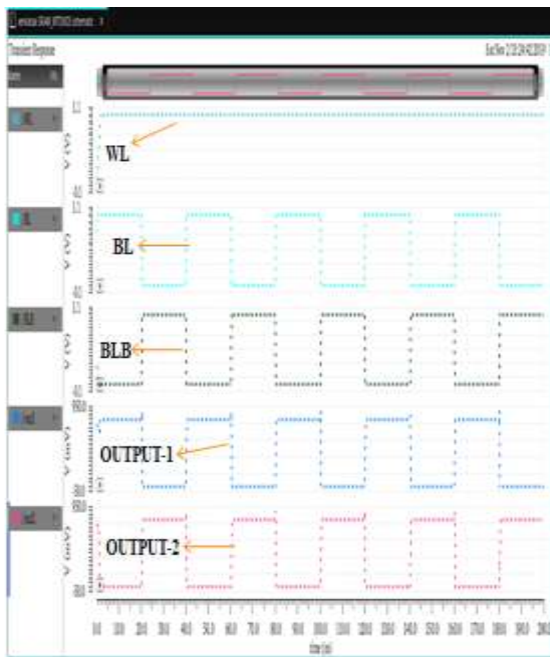

Fig 24: Transient response of MT-CMOS 8T SRAM cell

The stand by voltage is 1V and stand by bar voltage is 0V. There it provides high threshold voltage is to PMOS and NMOS transistors. Then the power gating process starts in circuit. Hence the power consumption is reduced.

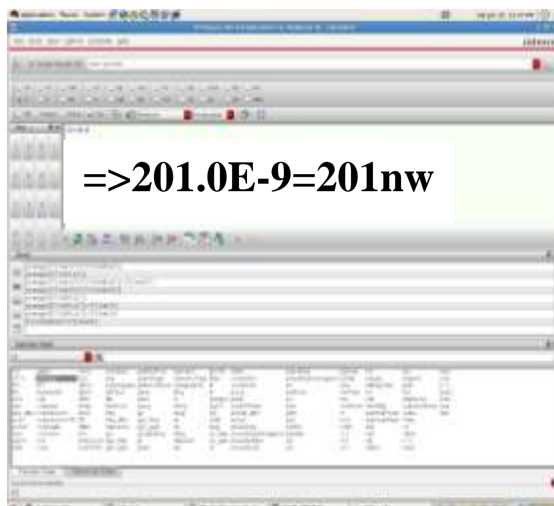

Fig 25: Power consumption MT-CMOS 8T SRAM cell

the power consumption of MT-CMOS 8T SRAM cell is 201.0nw.Hence the power consumption is decreased to 57% of the conventional 8T SRAM cell.

2.2 VARIABLE THRESHOLD CMOS TECHNIQUE

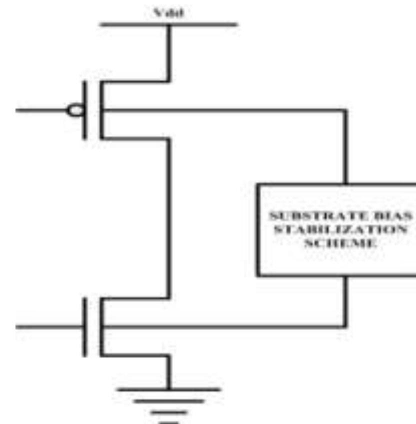

Fig 26: block diagram of VT-CMOS Technique

The threshold voltage of low V_t devices are varied by applying substrate bias voltage to achieve different substrate bias voltage levels at different parts of circuit.Reduction of the standby OFF current (I-OFF) while maintains the circuit speed.Substrate biasing in PMOS biases the body of transistor to a voltage higher than V_{dd}.In NMOS, to a voltage lower than Vss.

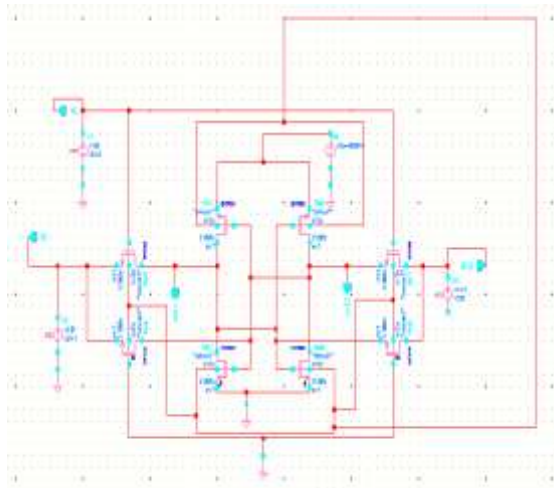

Fig 27: Schematic of VT-CMOS 8T SRAM cell

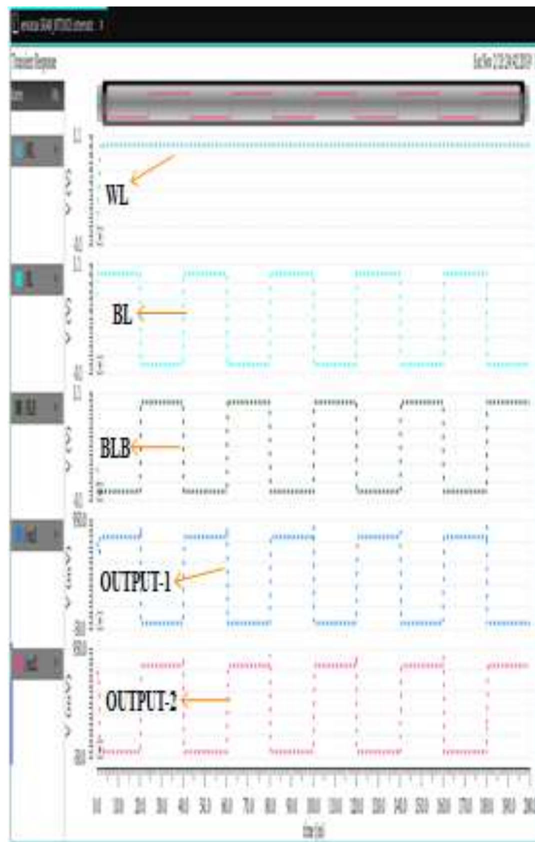

Fig 28: Transient response of VT-CMOS 8T SRAM cell

Fig 29: power consumption of VT-CMOS 8T SRAM cell

Thepower consumption of VT-CMOS 8T SRAM cell is 294.2nw.Hence the power consumption is decreased to 37% of the conventional 8T SRAM cell.

3. Comparison of SRAM cells

SRAM CELL	POWER CONSUMPTION (P_c)
Conventional 8T Symmetrical SRAM Cell	471.3nw
MT-CMOS 8T Symmetrical SRAM Cell	201.1nw
VT-CMOS 8T Symmetrical SRAM Cell	294.2nw

Table 2: Comparison of power consumption of SRAM cells

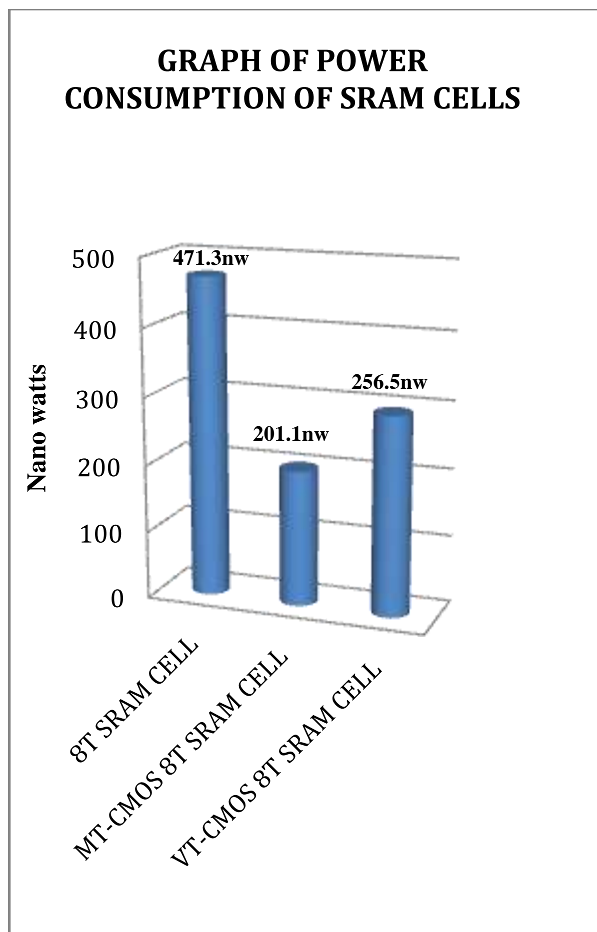

Fig: 30 Graph of power consumption of SRAM cells.

4. CONCLUSION

A Low power 8X8 SRAM array is designed for storing 64 bits. Peripheral components such as 3 to 8 decoder, Pre charge circuit, write driver circuit, sense amplifier including and has been designed and assembled to form SRAM array. Differential type sense amplifier is used for noise reduction. Pulse input signal with a peak to peak voltage of 800.0mV (rail-rail) and Supply voltage of 800.0mV for SRAM cells and for 8×8 SRAM array the supply voltage is 1.8V is considered Transient responses for read and write operations for both logic-1 and logic-0 have been analyzed.Investigated the low power techniques such as MTCMOS and VTCMOS in 8T SRAM cell.Among two techniques better results got in MTCMOS Technique.In this Technique reducing the power consumption to 57% as compared to conventional 8T symmetrical SRAM cell. SRAM array and SRAM cells and peripheral components are designed in Cadence toolswith 180nm CMOS Technology.

5. References

[1] Robert Giterman, MaozVicentowski, Itamar Levi, YoavWeizman, OsnatKeren and Alexander Fish., “Leakage Power Attack-Resilient Symmetrical 8T SRAM Cell,” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS”, no.5, May. 2018.

[2] E. Seevinck et al., “Static-Noise Margin Analysis of MOS SRAMCells,” IEEE J.Solid-State Circuits, vol.SC-22, no.5 pp.748-754,
Oct. 1987.

[3] Benton H. Calhaun, Anantha P. Chandrakasan “Static Noise MarginVariation for Sub-threshold SRAM in 65 nm CMOS”, IEEE Journalof Solid-State Circuits,, pp.1673-1679. vol.41,July 2006.

[4] Benton H. Calhoun Anantha P. andrakasan, “Analyzing StaticNoise Margin for Sub-thresholdSRAM in65nmCMOS”,ESSCIRC,2005.

[5] S. Tavva et al. “Variation Tolerant 9T SRAM Cell Design”GLSVLSI“10,pp.55-60,may 16, 2010.

[6] Arandilla,C.D.C et al.“Static Noise Margin of 6T SRAM Cell in 90-nm CMOS” IEEE 13th International Conference on computer modeling and Simulation, pp.534-539,March 30,2011.

[7] K. S. Yeo, W. L. Goh, Z. H. Kong, Q. X. Zhang, andW. G Yeo, “High-performance low-power currentsense amplifier using a cross-coupled current-mirrorconfiguration,” IEE Proc. G Circuits, Devices, andSystems, Vol. 149, No. 56, pp. 308-314, Oct. 2002.

[8] Singh S K, Singh S V, Kausik B K, Chauhan C and Tripathi T 2014 Characteriztion& improvement of SNM in deep submicron SRAM design International Conference on Signal Processing and Integrated Networkspp 538-542.

[9] Christiensen D.C. Arandilla, Anastacia B. Alvarez and Christian Raymund K. Roque 2011 Static noise margin of 6T SRAM cell in 90-nm CMOS International Conference on Modelling and Simulationpp 534-539.

[10] VanamaKundan, GunnuthulaRithwik and Prasad Govind 2014 Design of low power stable SRAM cell International Conference on Circuit, Power and Computing Technologies pp 1263-1267.

[11] Banga H and Agarwal D 2017 Single bit-line 10T SRAM cell for low power and high SNM International Conference on Recent Innovation in Signal Processing and Embedded Systemspp433-438.

[12] Kumar C A et al. 2016 Performance analysis of low power 6T SRAM cell in 180nm and 90nm International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics pp 1-7.